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SPECIFICATION

CUSTOMER ： _____

MODULE NO.: WO12864-xxxD1#FC

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General Specification

Item	Dimension	Unit
Number of Characters	128 x 64 dots	—
Module dimension	80.0x 54.0 x10.2(MAX)	mm
View area	70.7 x 38.8	mm
Active area	66.52 x 33.24	mm
Dot size	0.48 x0.48	mm
Dot pitch	0.52 x 0.52	mm

Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_{OP}	-20	—	+70	℃
Storage Temperature	T_{ST}	-30	—	+80	℃
Input Voltage	V_I	-0.3	—	V_{DD}+0.3	V
Supply Voltage For Logic	V_{DD}-V_{SS}	-0.3		5.0	V
LCD Driver Supply Voltage	V_{OUT}	4		13	V

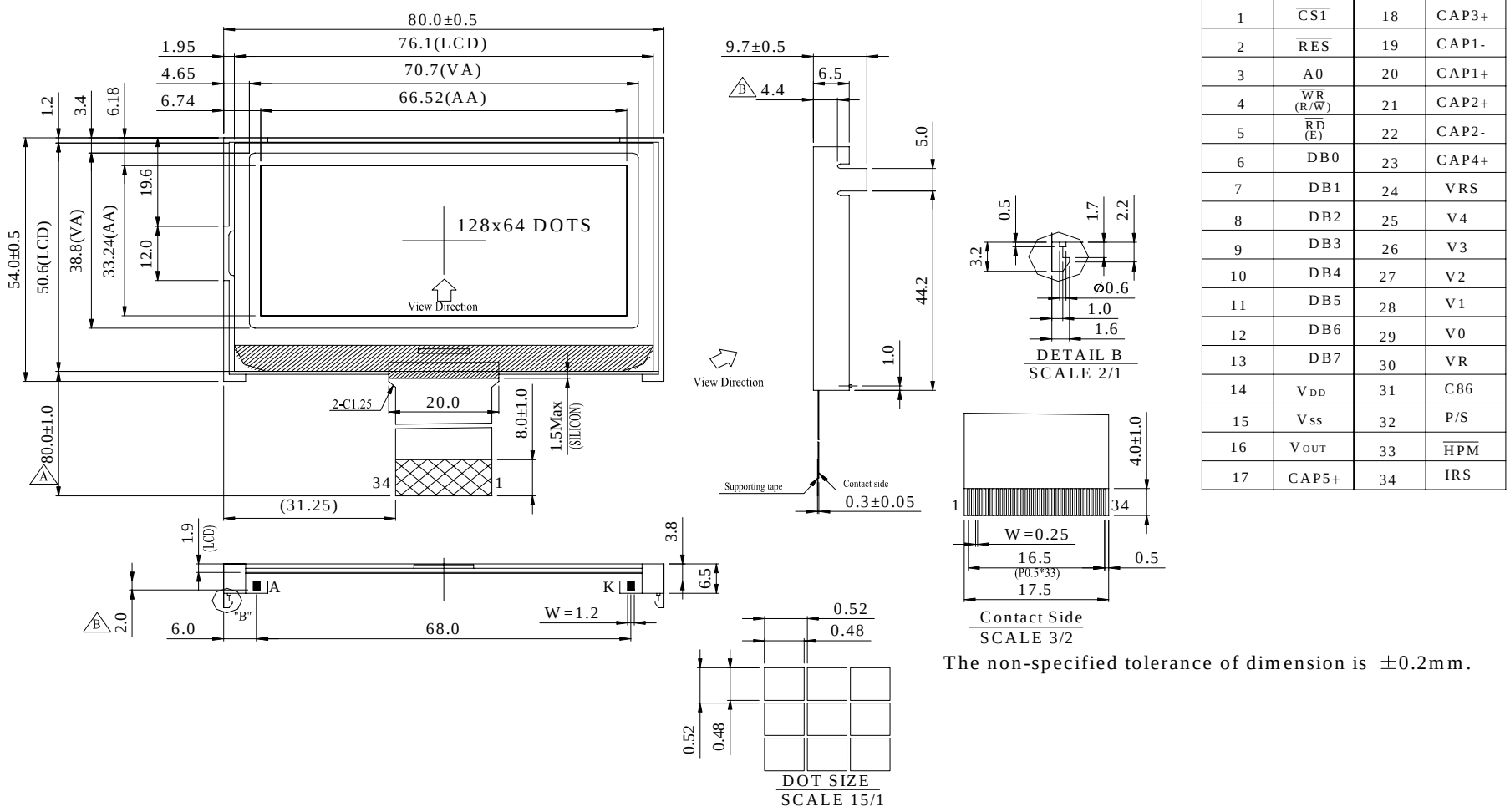
Interface Pin Function

Pin No.	Symbol	Level	Description
1	/CS1		This is the chip select signal. When /CS1 = "L" , then the chip select becomes active, and data/command I/O is enabled.
2	/RES		When /RES is set to "L" , the settings are initialized.
3	A0		This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = "H" : Indicates that D0 to D7 are display data. A0 = "L" : Indicates that D0 to D7 are control data.
4	/WR(R/W)		When connected to an 8080 MPU, this is active LOW. (R/W) This terminal connects to the 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When R/W = "H" : Read. When R/W = "L" : Write.
5	/RD(E)		When connected to an 8080 MPU, this is active LOW. (E) This pin is connected to the /RD signal of the 8080 MPU, and the ST7565P series data bus is in an output status when this signal is "L" . When connected to a 6800 Series MPU, this is active HIGH. This is the 6800 Series MPU enable clock input terminal.
6	DB0		This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data Bus.
7	DB1		
8	DB2		
9	DB3		
10	DB4		
11	DB5		
12	DB6		
13	DB7		
14	VDD		Shared with the MPU power supply terminal VDD. (3.3 V)
15	VSS		This is a 0V terminal connected to the system GND.
16	VOUT		DC/DC voltage converter. Connect a capacitor between this terminal and VSS.
17	CAP5+		DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
18	CAP3+		DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.

<table>
<tr><td>19</td><td>CAP1-</td><td></td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.</td></tr>
<tr><td>20</td><td>CAP1+</td><td></td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.</td></tr>
<tr><td>21</td><td>CAP2+</td><td></td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.</td></tr>
<tr><td>22</td><td>CAP2-</td><td></td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal.</td></tr>
<tr><td>23</td><td>CAP4+</td><td></td><td>DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.</td></tr>
<tr><td>24</td><td>VRS</td><td></td><td>This is the externally-input VREG power supply for the LCD power supply voltage regulator.</td></tr>
<tr><td>25</td><td>V4</td><td></td><td rowspan="5">This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on Vss, and must maintain the relative magnitudes shown below.
V0 ≧V1 ≧V2 ≧V3 ≧V4 ≧Vss
When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.
<table><tr><td></td><td>1/65 DUTY</td><td>1/49 DUTY</td><td>1/33 DUTY</td><td>1/55 DUTY</td><td>1/53 DUTY</td></tr><tr><td>V1</td><td>8/9*V0,6/7*V0</td><td>7/8*V0,5/6*V0</td><td>5/6*V0,4/5*V0</td><td>7/8*V0,5/6*V0</td><td>7/8*V0,5/6*V0</td></tr><tr><td>V2</td><td>7/9*V0,5/7*V0</td><td>6/8*V0,4/6*V0</td><td>4/6*V0,3/5*V0</td><td>6/8*V0,4/6*V0</td><td>6/8*V0,4/6*V0</td></tr><tr><td>V3</td><td>2/9*V0,2/7*V0</td><td>2/8*V0,2/6*V0</td><td>2/6*V0,2/5*V0</td><td>2/8*V0,2/6*V0</td><td>2/8*V0,2/6*V0</td></tr><tr><td>V4</td><td>1/9*V0,1/7*V0</td><td>1/8*V0,1/6*V0</td><td>1/6*V0,1/5*V0</td><td>1/8*V0,1/6*V0</td><td>1/8*V0,1/6*V0</td></tr></table></td></tr>
<tr><td>26</td><td>V3</td><td></td></tr>
<tr><td>27</td><td>V2</td><td></td></tr>
<tr><td>28</td><td>V1</td><td></td></tr>
<tr><td>29</td><td>V0</td><td></td></tr>
<tr><td>30</td><td>VR</td><td></td><td>Output voltage regulator terminal. Provides the voltage between VDD and V5 through a resistive voltage divider.
IRS = “L” : the V5 voltage regulator internal resistors are not used .
IRS = “H” : the V5 voltage regulator internal resistors are used .</td></tr>
<tr><td>31</td><td>C86</td><td></td><td>This is the MPU interface switch terminal.
C86 = “H”: 6800 Series MPU interface.
C86 = “L”: 8080 MPU interface.</td></tr>
<tr><td>32</td><td>P/S</td><td></td><td>This is the parallel data input/serial data input switch terminal.
P/S = “H”: Parallel data input.
P/S = “L”: Serial data input.
The following applies depending on the P/S status:
<table><tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr><tr><td>“H”</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$, $\overline{WR}$</td><td>X</td></tr><tr><td>“L”</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr></table>When P/S = “L”, D0 to D5 may be “H”, “L” or Open. RD (E) and WR (R/W) are fixed to either “H” or “L”. With serial data input, It is impossible read data from RAM .</td></tr>
<tr><td>33</td><td>/HPM</td><td></td><td>This is the power control terminal for the power supply circuit for liquid crystal drive.
HPM = “H”: Normal mode
HPM = “L”: High power mode</td></tr>
</table>

34	IRS		This terminal selects the resistors for the V5 voltage level adjustment. IRS = "H" : Use the internal resistors IRS = "L" : Do not use the internal resistors. The V5 voltage level is regulated by an external resistive voltage divider attached to the VR terminal

Contour Drawing &Block Diagram



PIN NO.	SIGNAL	PIN NO.	SIGNAL
1	$\overline{CS1}$	18	CAP3+
2	$\overline{RES}$	19	CAP1-
3	A0	20	CAP1+
4	$\overline{WR}$ (R/$\overline{W}$)	21	CAP2+
5	$\overline{RD}$ ($\overline{E}$)	22	CAP2-
6	DB0	23	CAP4+
7	DB1	24	VRS
8	DB2	25	V4
9	DB3	26	V3
10	DB4	27	V2
11	DB5	28	V1
12	DB6	29	V0
13	DB7	30	VR
14	V_{DD}	31	C86
15	Vss	32	P/S
16	V_{OUT}	33	$\overline{HPM}$
17	CAP5+	34	IRS

The non-specified tolerance of dimension is ±0.2mm.