Next Vision Display
Brighten The Future

NEXT VISION DISPLAY

SPECIFICATION

CUSTOMER : _____

MODULE NO.: NE058-N001GD

Version	
Engineer	
Date	

Customer:
Approved by

Next Vision Display
Brighten The Future

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1. General Description

1.1 Over View

The display is a TFT active matrix electrophoretic display, with interface and a reference system design. The 5.83" active area contains 600×448 pixels, and has 1-bit white/black full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

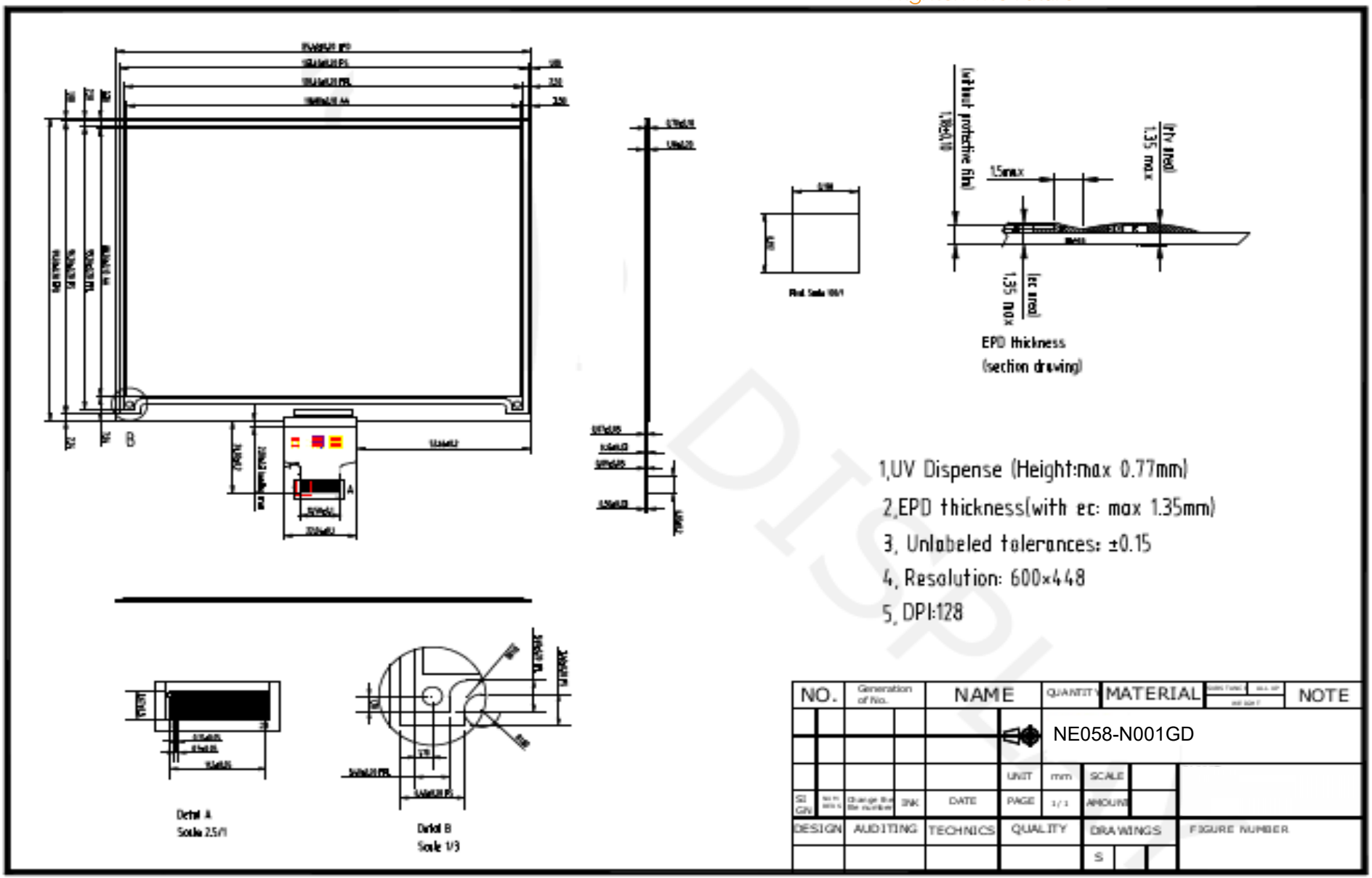
1.2 Features

- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape, portrait mode
- Antiglare hard-coated front-surface
- Low current sleep mode
- On chip display RAM
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and source driving voltage
- I^2C Signal Master Interface to read external temperature sensor
- Available in COG package IC thickness 280um

1.3 Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	5.83	Inch	
Display Resolution	600(H) × 448(V)	Pixel	Dpi:128
Active Area	118.80(H) × 88.26(V)	mm	
Pixel Pitch	0.198 × 0.197	mm	
Pixel Configuration	Rectangle		
Outline Dimension	125.40(H) × 99.50(V) × 1.18(D)	mm	
Weight	28±0.5	g	

1.4 Mechanical Drawing of EPD module



1.5 Input/Output Terminals

Pin #	Type	Single	Description	Remark
1	I	MFCSB	Serial communication chip select. It would bypass to MFCSB by R61H command.	
2	O	GDR	N-Channel MOSFET Gate Drive Control	
3	O	RESE	Current Sense Input for the Control Loop	
4	C	VGL	Negative Gate driving voltage	
5	C	VGH	Positive Gate driving voltage	
6	O	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	I/O	TSDA	I2C Interface to digital temperature sensor Date pin	
8	I	BS1	Bus selection pin	Note 1.5-5
9	O	BUSY	Busy state output pin	Note 1.5-4
10	I	RES #	Reset	Note 1.5-3
11	I	D/C #	Data /Command control pin	Note 1.5-2
12	I	CS #	Chip Select input pin	Note 1.5-1
13	I/O	D0	serial clock pin (SPI)	
14	I/O	D1	serial data pin (SPI)	
15	I	VDDIO	Power for interface logic pins	
16	I	VCI	Power Supply pin for the chip	
17		VSS	Ground	
18	C	VDD	Core logic power pin	
19	O	FMSDO	Serial communication data output. It would bypass to FMSDO by R61H command.	
20	C	VSH	Positive Source driving voltage	
21	C	PREVGH	Power Supply pin for VGH and VSH	
22	C	VSL	Negative Source driving voltage	
23	C	PREVGL	Power Supply pin for VCOM, VGL and VSL	
24	C	VCOM	VCOM driving voltage	

Note 1.5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled Low.

Note 1.5-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled High, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note 1.5-3: This pin (RES#) is reset signal input. The Reset is active Low.

Note 1.5-4: This pin (BUSY) is Busy state output pin. When Busy is Low the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin Low when the driver IC is working such as:

- Outputting display waveform; or
- Communicating with digital temperature sensor

Note 1.5-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is "Low", 4-line SPI is selected. When it is "High", 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

Table: Bus interface selection

BS1	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) – 9 bits

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