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NEXT VISION DISPLAY

SPECIFICATION

CUSTOMER : _____

MODULE NO.: NE027-N002GD

Version	1.0
Engineer	
Date	2021/10/12

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Customer:
Approved by

NEXT VISION DISPLAY CO., LTD.

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Overview

Active Matrix Electrophoretic Display (AM EPD) with interface and ,
a reference system design. The display is capable to display images at 1-bit white, black full display capabilities. The 2.66 inch active area contains 296×152 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2.Features

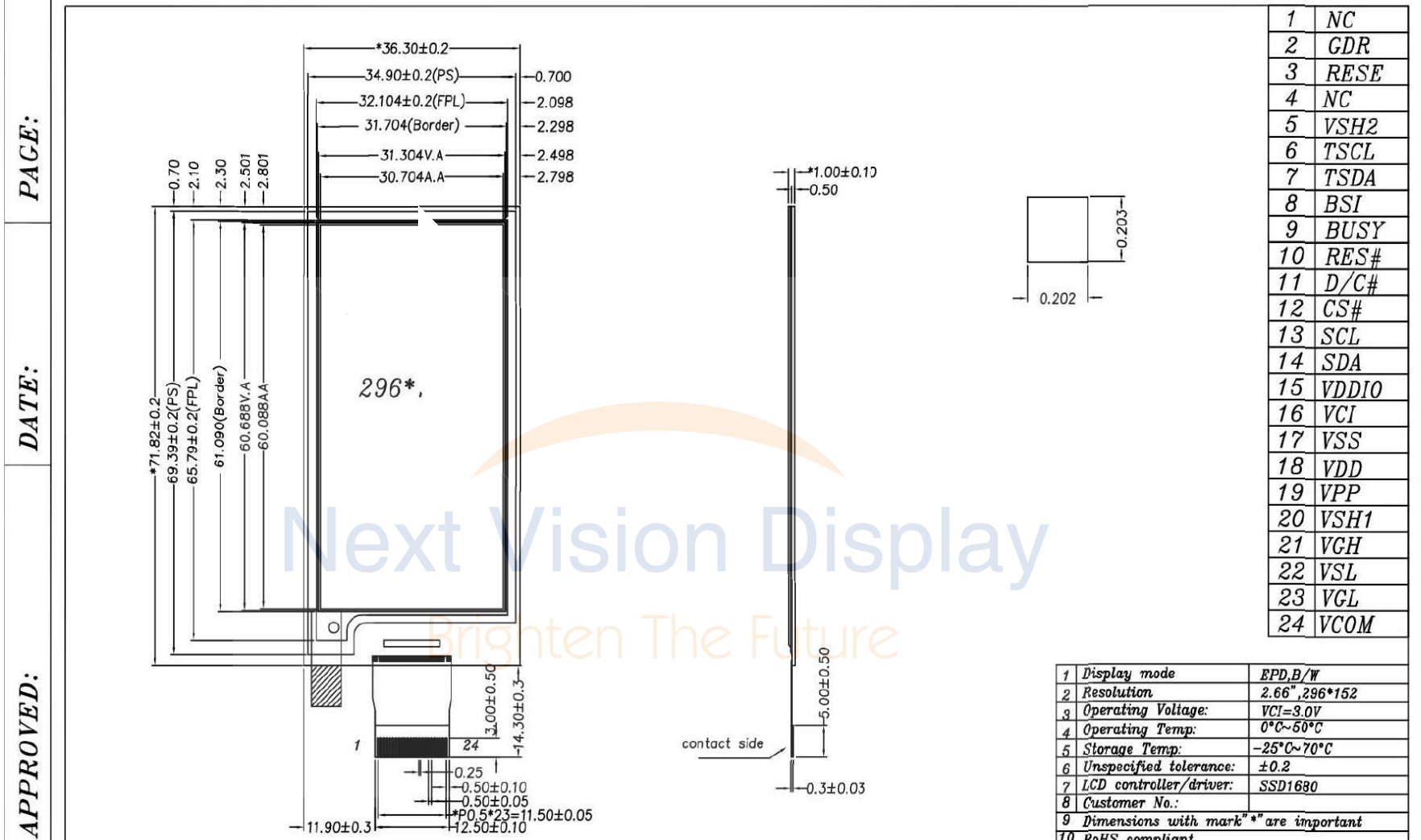
- 296×152 pixels display
- High contrast High reflectance
- Ultra wide viewing angle Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform can stored in On-chip OTP or written by MCU
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage

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3.Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.66	Inch	
Display Resolution	152(H)×296(V)	Pixel	Dpi:125
Active Area	30.704×60.088	mm	
Pixel Pitch	0.202×0.203	mm	
Pixel Configuration	Rectangle		
Outline Dimension	36.30(H)×71.82(V) ×1.0(D)	mm	
Weight	4.7±0.5	g	

Mechanical Drawing of EPD module



1	NC
2	GDR
3	RESE
4	NC
5	VSH2
6	TSCL
7	TSDA
8	BSI
9	BUSY
10	RES#
11	D/C#
12	CS#
13	SCL
14	SDA
15	VDDIO
16	VCI
17	VSS
18	VDD
19	VPP
20	VSH1
21	VGH
22	VSL
23	VGL
24	VCOM

1	Display mode	EPD,B/W
2	Resolution	2.66",296*152
3	Operating Voltage:	VCI=3.0V
4	Operating Temp:	0°C~50°C
5	Storage Temp:	-25°C~70°C
6	Unspecified tolerance:	±0.2
7	LCD controller/driver:	SSD1680
8	Customer No.:	
9	Dimensions with mark"*"are important	
10	RoHS compliant	

NO.	DESCRIPTION	NAME	DATE
3			
2			
1			
	Initial version	WJZ	2021/10/12

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Drw
Chk
Apv
Unit:mm

PAGE:
DATE:
CUSTOMER'S APPROVED:

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Input /Output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage(Red)	
6	TSCL	O	I^2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I^2C Interface to digital temperature sensor Data pin	
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

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I = Input Pin, O =Output Pin, /O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when -Outputting display waveform -Communicating with digital temperature sensor.

Note 5-5: Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

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Electrical Characteristics

Absolute maximum rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.5 to +4.0	V
Logic Input voltage	VIN	-0.5 to VCI +0.5	V
Logic Output voltage	VOUT	-0.5 to VCI +0.5	V
Operating Temp range	TOPR	0 to +50	°C
Storage Temp range	TSTG	-25 to+70	°C
Optimal Storage Temp	TSTGo	23±2	°C
Optimal Storage Humidity	HSTGo	55±10	%RH

Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

7.2. Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25ºC

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Single ground	V_{SS}	-		-	0	-	V
Logic supply voltage	V_{CI}	-	VCI	2.2	3.0	3.7	V
Core logic voltage	V_{DD}		VDD	1.7	1.8	1.9	V
High level input voltage	V_{IH}	-	-	0.8 V_{CI}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2 V_{CI}	V
High level output voltage	V_{OH}	IOH = - 100uA	-	0.9 VCI	-	-	V
Low level output voltage	V_{OL}	IOL = 100uA	-	-	-	0.1 V_{CI}	V
Typical power	P_{TYP}	V_{CI} =3.0V	-	-	TBD	-	mW
Deep sleep mode	P_{STPY}	V_{CI} =3.0V	-	-	0.003	-	mW
Typical operating current	Iopr_V_{CI}	V_{CI} =3.0V	-	-	TBD	-	mA
Full update time	-	25 ºC	-	-	3	-	sec
Fast update time	-	25 ºC	-	-	1.5	-	sec
Partial update time	-	25 ºC	-	-	0.42	-	sec
Sleep mode current	Islp_V_{CI}	DC/ DC off No clock No input load Ram data retain	-	-	20		uA
Deep sleep mode current	Idslp_V_{CI}	DC/ DC off No clock No input load Ram data not retain	-	-	2	6	uA

Notes:
1) Refresh time: the time it takes for the whole process from the screen change to the screen stabilization.

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2) The difference between different refresh methods:

Full refresh: The screen will flicker several times during the refresh process;

Fast Refresh: The screen will flash once during the refresh process;

Partial refresh: The screen does not flicker during the refresh process.

Note: During the fast refresh or partial refresh of the electronic paper, it is recommended to add a full-screen refresh after 5 consecutive operations to reduce the accumulation of afterimages on the screen.

Notes: 1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.

2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Good Display.

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7.3. Panel AC Characteristics

7.3.1. MCU Interface

The pin assignment at different interface mode is summarized in Table 7.4.1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

7.3.2. MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

Note:

In the write mode SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte . The data byte in the shift register is written to the Graphic Display Data RAM /Data Byte register or command Byte register according to D/C# pin.

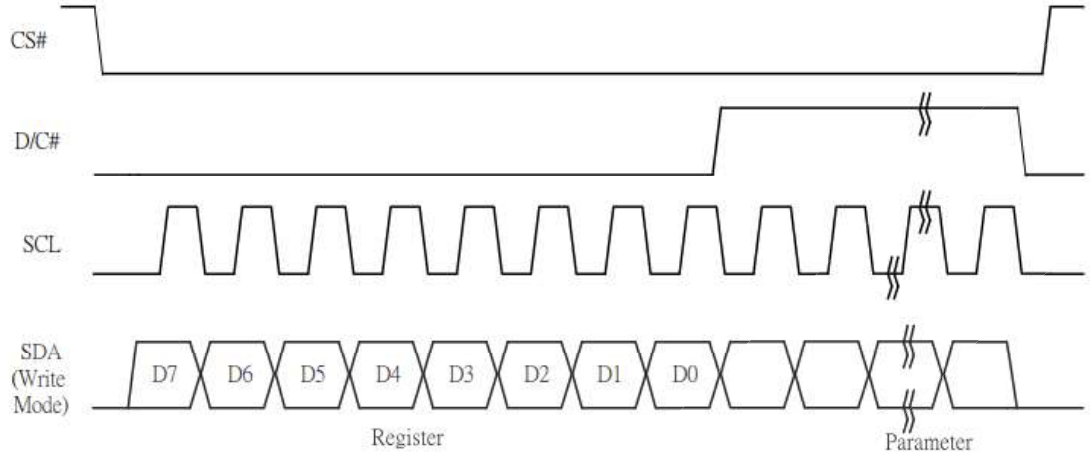


Figure 7-1 : Write procedure in 4-wire SPI mode

In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0 with D/C# keep low.
3. After SCL change to low for the last bit of register, D/C# need to drive to high.
4. SDA is shifted out an 8-bit data on every falling adge of SCL in the order of D7, D6, ... D0.
5. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

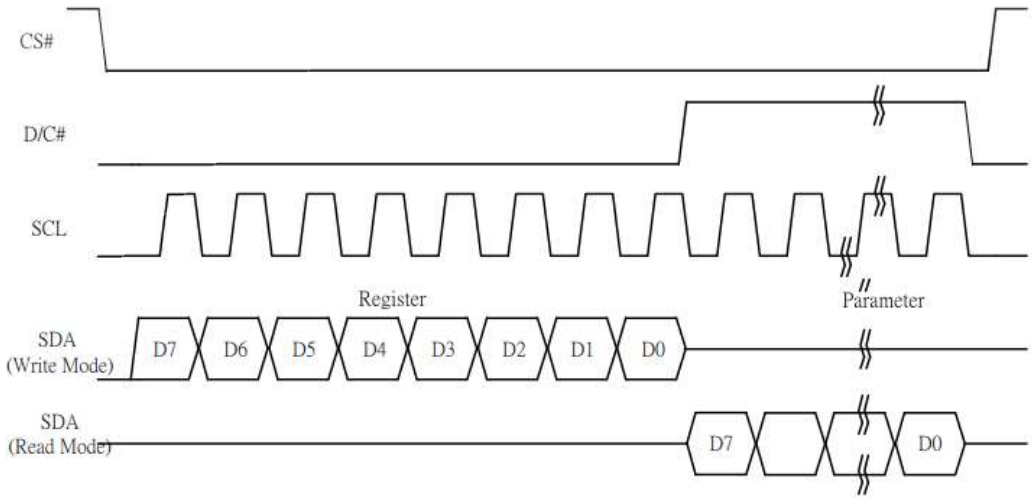


Figure 7-2 : Read procedure in 4-wire SPI mode

7.3.3. MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCL, serial data SDA and CS#. This interface also supports Write mode and Read mode.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

nction	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

Note： ↑ stands for rising edge of signal

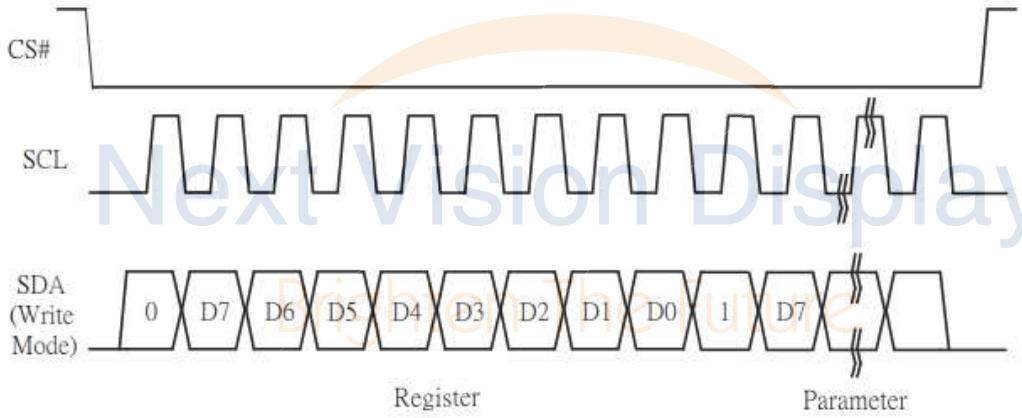


Figure 7-3 : Write procedure in 3-wire SPI

In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.

2. D/C=0 is shifted thru SDA with one rising edge of SCL

3. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0.

4. D/C=1 is shifted thru SDA with one rising edge of SCL

5. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, … D0.

6. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

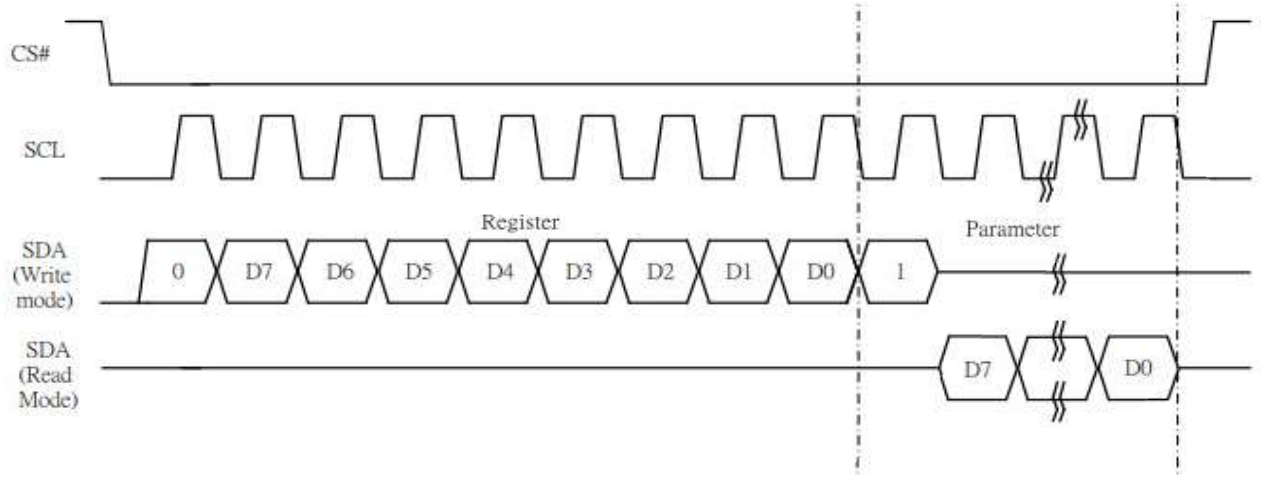
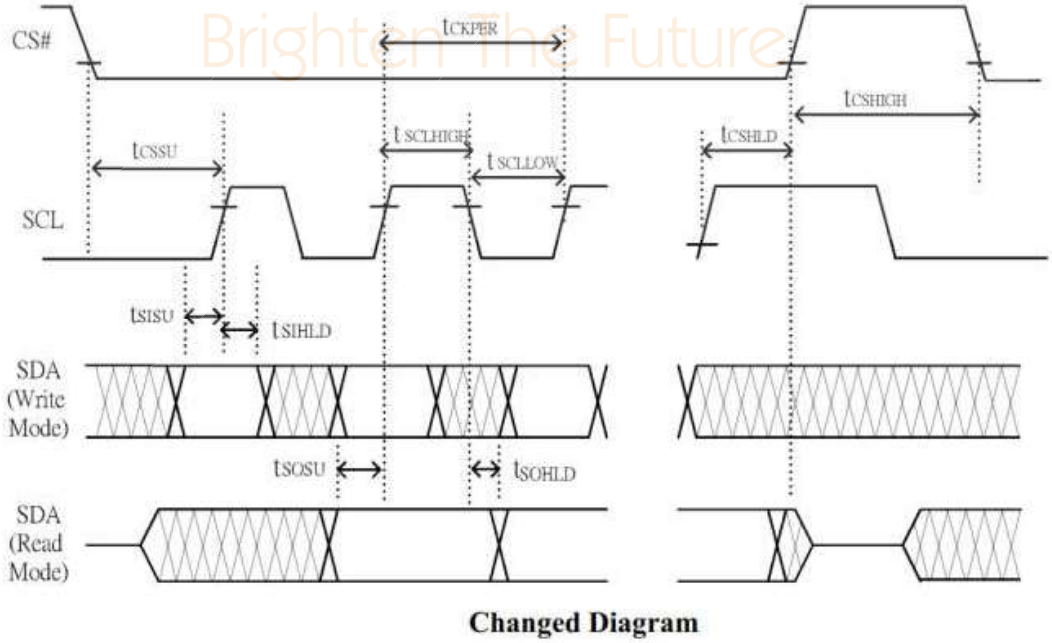


Figure 7-4 : Read procedure in 3-wire SPI mode

7.3.4. Interface Timing

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25ºC.



Changed Diagram

Serial Interface Timing Characteristics

(VIC - VSS = 2.2V to 3.7V, TOPR = 25℃, CL = 20pF

Optical Specifications

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	8-1
CR	Contrast Ratio	Indoor	8:1		-		8-2
GN	2Grey Level	-		DS+(WS-DS)*n(m-1)			8-3
T update	Image update time	at 25 °C		3	-	sec	
Life		Topr		1000000times or 5years			

Notes:

8-1. Luminance meter: Eye-One Pro Spectrophotometer.

8-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

8-3. WS: White state, DS: Dark state

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