Winstar Display Co., LTD
華凌光電股份有限公司
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SPECIFICATION

MODULE NO.: WF123-1920720BL#0SPW0-FC

General Specifications

Item	Dimension	Unit
Size	12.3	inch
Pixel Number	1920 RGB (H) x 720(V)	pixel
Module dimension	308.1(H) x 130.0(V) x7.6	mm
Active Area	292.032(H) x 109.512(V)	mm
Pixel Pitch	0.1521(H) x 0.1521 (V)	mm
LCD type	TFT, Normally Black, Transmissive	
Viewing Angle	85/85/85/85	
Backlight Type	LED, Normally White	
TFT Interface	2ch-LVDS	
Touch Panel	Without Touch Panel	
Surface	Anti-Glare	

*Color tone slight changed by temperature and driving voltage.

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Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-30	—	+85	℃
Storage Temperature	TST	-40	—	+90	℃

Electrical Characteristics

TFT LCD Module

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	3	3.3	3.6	V
Input signal voltage	ViH	VCC *0.7	-	VCC	V
	ViL	0	-	VCC *0.3	V
Current of power supply	ICC	--	--	500	mA

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Interface

TFT LCD MODULE

FPC connector is used for electronics interface.
AORORA F31L-1A7H1-21050 , 50PIN

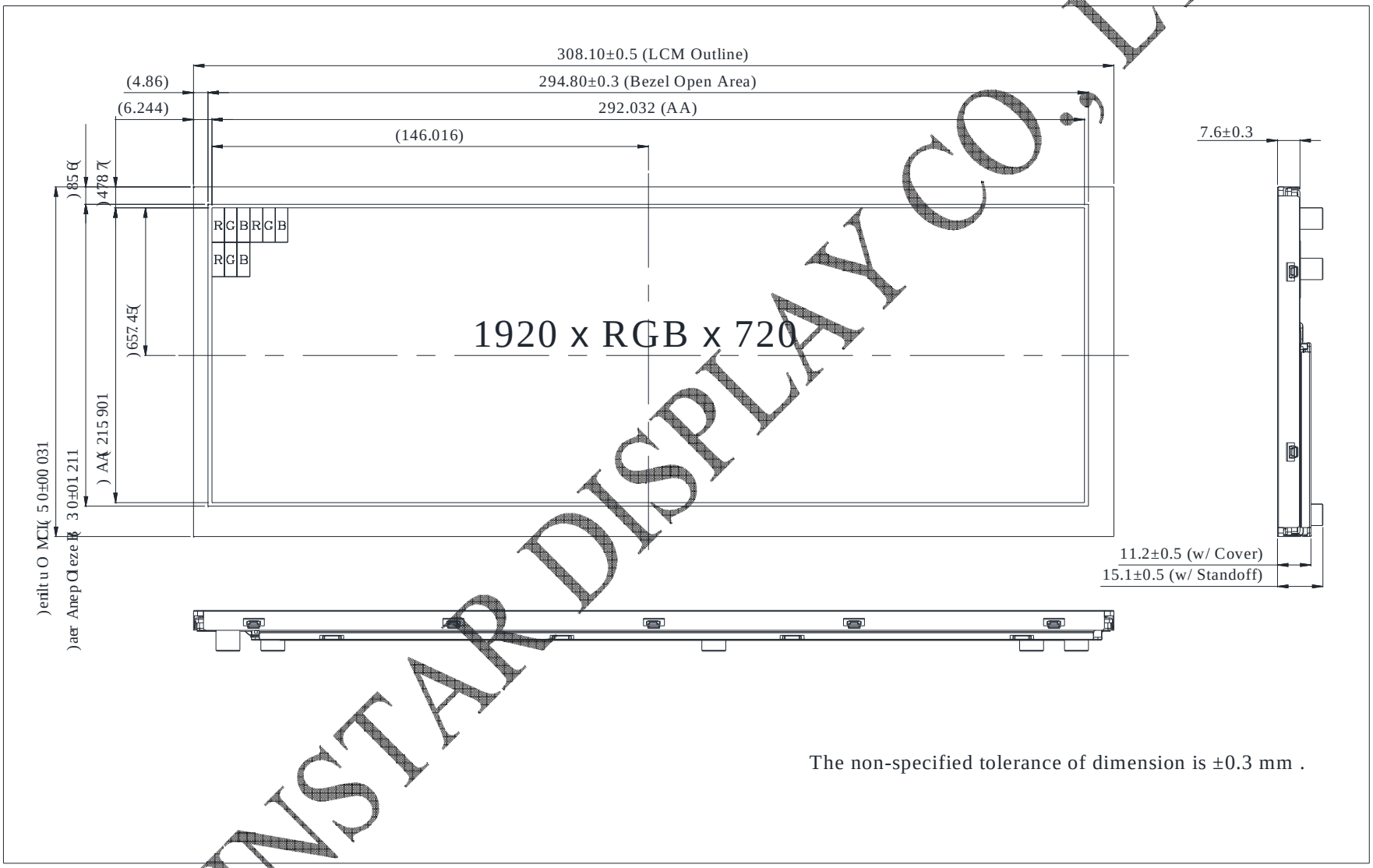
Pin no.	Symbol	Function
1	GND	Ground
2	NC	No connector
3	VCC	Digital Power
4	VCC	Digital Power
5	GND	Panel Power
6	GND	Panel Power
7	NC	No connector
8	NC	No connector
9	GND	Ground
10	ORXIN0-	Odd pixel negative LVDS differential clock input
11	ORXIN0+	Odd pixel positive LVDS differential clock input
12	ORXIN1-	Odd pixel negative LVDS differential clock input
13	ORXIN1+	Odd pixel positive LVDS differential clock input
14	ORXIN2-	Odd pixel negative LVDS differential clock input
15	ORXIN2+	Odd pixel positive LVDS differential clock input
16	ORXCLKIN-	Odd pixel negative LVDS differential clock input
17	ORXCLKIN+	Odd pixel positive LVDS differential clock input
18	ORXIN3-	Odd pixel negative LVDS differential clock input
19	ORXIN3+	Odd pixel positive LVDS differential clock input
20	ERXIN0-	Even pixel negative LVDS differential clock input
21	ERXIN0+	Even pixel positive LVDS differential clock input
22	ERXIN1-	Even pixel negative LVDS differential clock input
23	ERXIN1+	Even pixel positive LVDS differential clock input
24	ERXIN2-	Even pixel negative LVDS differential clock input
25	ERXIN2+	Even pixel positive LVDS differential clock input
26	ERXCLKIN-	Even pixel negative LVDS differential clock input
27	ERXCLKIN+	Even pixel positive LVDS differential clock input
28	ERXIN3-	Even pixel negative LVDS differential clock input
29	ERXIN3+	Even pixel positive LVDS differential clock input

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30	GND	Ground
31	NC	No connector
32	RESETB	Global reset pin, active low.
33	STBYB	Standby mode, active low.
34	CA3	Output signal to indicate self protection mode, when DE,HS,VS,DCLK, any of these signals is missing, it will become High. If using this pin, CA3 need to pulled low by an resistor,else , let it floating.
35	SCL	Serial interface clock input. (User folating)
36	SDA	Serial interface data input/output.(User folating)
37	CSB	Serial interface chip enable.(User folating)
38	GND	Power Ground
39	GND	Power Ground
40	NC	No connector
41	LEDA	LED power (Anode)
42	LEDA	LED power (Anode)
43	LEDA	LED power (Anode)
44	NC	No connector
45	LEDK1	Cathode 1
46	LEDK2	Cathode 2
47	LEDK3	Cathode 3
48	LEDK4	Cathode 4
49	NTC_A	NTC_Anode
50	NTC_K	NTC_Cathode

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Contour Drawing

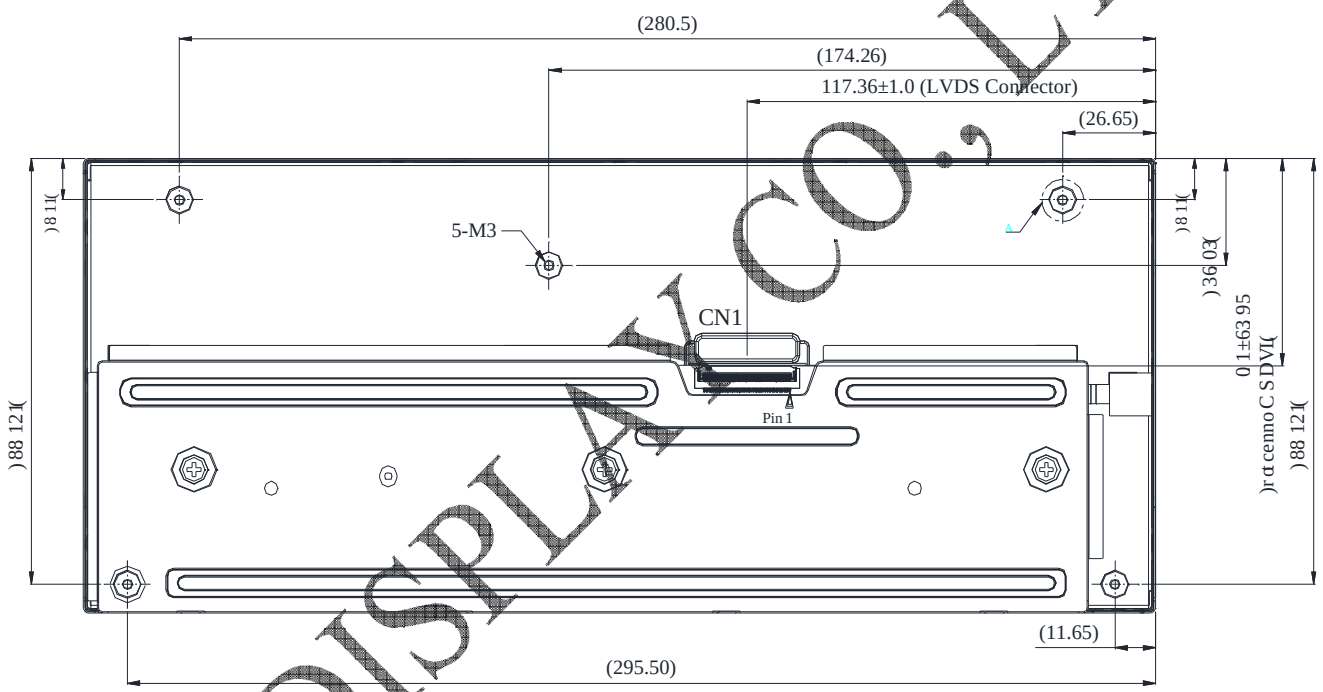


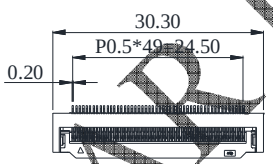
The non-specified tolerance of dimension is ±0.3 mm .

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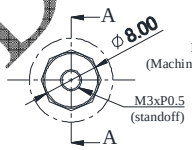
CN1(F31L-1A7H1-21050)

PIN NO	SYMBOL	PIN NO	SYMBOL
1	GND	29	ERXIN3+
2	NC	30	GND
3	VCC	31	NC
4	VCC	32	RESETB
5	GND	33	STBYB
6	GND	34	CA3
7	NC	35	SCL
8	NC	36	SDA
9	GND	37	CSB
10	ORXIN0-	38	GND
11	ORXIN0+	39	GND
12	ORXIN1-	40	NC
13	ORXIN1+	41	LEDA
14	ORXIN2-	42	LEDA
15	ORXIN2+	43	LEDA
16	ORXCLKIN-	44	NC
17	ORXCLKIN+	45	LEDK1
18	ORXIN3-	46	LEDK2
19	ORXIN3+	47	LEDK3
20	ERXIN0-	48	LEDK4
21	ERXIN0+	49	NTC_A
22	ERXIN1-	50	NTC_K
23	ERXIN1+		
24	ERXIN2-		
25	ERXIN2+		
26	ERXCLKIN-		
27	ERXCLKIN+		
28	ERXIN3-		

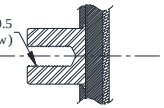




F31L-1A7H1-21050
SCALE 2/1



DETAIL A
SCALE 2:1
TOTAL 5



SECTION A-A
SCALE 2:1
TOTAL 5

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