TFT DISPLAY SPECIFICATION



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SPECIFICATION

MODULE NO.: WFN0286DA2#0SPW15-FC

General Specifications

Item	Dimension	Unit
Size	2.86	inch
Dot Matrix	376 x RGB x 960 (TFT)	dots
Module dimension	40.2 (W) x 84.3 (H) x 3.85 (D)	mm
Active area	26.508 x 67.68	mm
Pixel Pitch	0.0705 x 0.0705	mm
LCD type	TFT, Normally Black, Transmissive	
Viewing angle	85/85/85/85	
Aspect Ratio	1：2.5	
TFT Interface	3W SPI+RGB24bit	
TFT Driver IC	ST7701P or Equivalent	
CTP Driver IC	ST1633i or equivalent	
CTP Interface	I2C	
CTP FW Version	0x02	
CTP Resolution	376x960	
Touch Panel	Projected Capacitive Touch Panel (PCAP)	
Backlight Type	LED, Normally White	
Surface	Glare	

*Color tone slight changed by temperature and driving voltage.

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Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-30	—	+85	℃
Storage Temperature	TST	-30	—	+85	℃

Electrical Characteristics

1. Operating conditions

Item	Symbol	Min	Typ	Max	Unit
Interface Supply Voltage	VCC	2.5	2.8	3.3	V
Current for Drive	IVCC	—	25	40	mA
Input voltage 'H' level	VIH	0.7*VCC	—	VCC	V
Input voltage 'L' level	VIL	GND	—	0.3*VCC	V
Output voltage 'H' level	VOH	0.8* VCC	—	VCC	V
Output voltage 'L' level	VOL	GND	—	0.2* VCC	V
Supply CTP	TP_VDDT	3.0	3.3	3.6	V
	TP_IDDT	—	2.6	4.0	mA

2. LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
LED current	—	—	30	—	mA
LED voltage	VLED+	15.5	17.0	18.5	V
LED Life Time	—	50,000	—	—	Hr

Interface

1. LCM PIN Definition

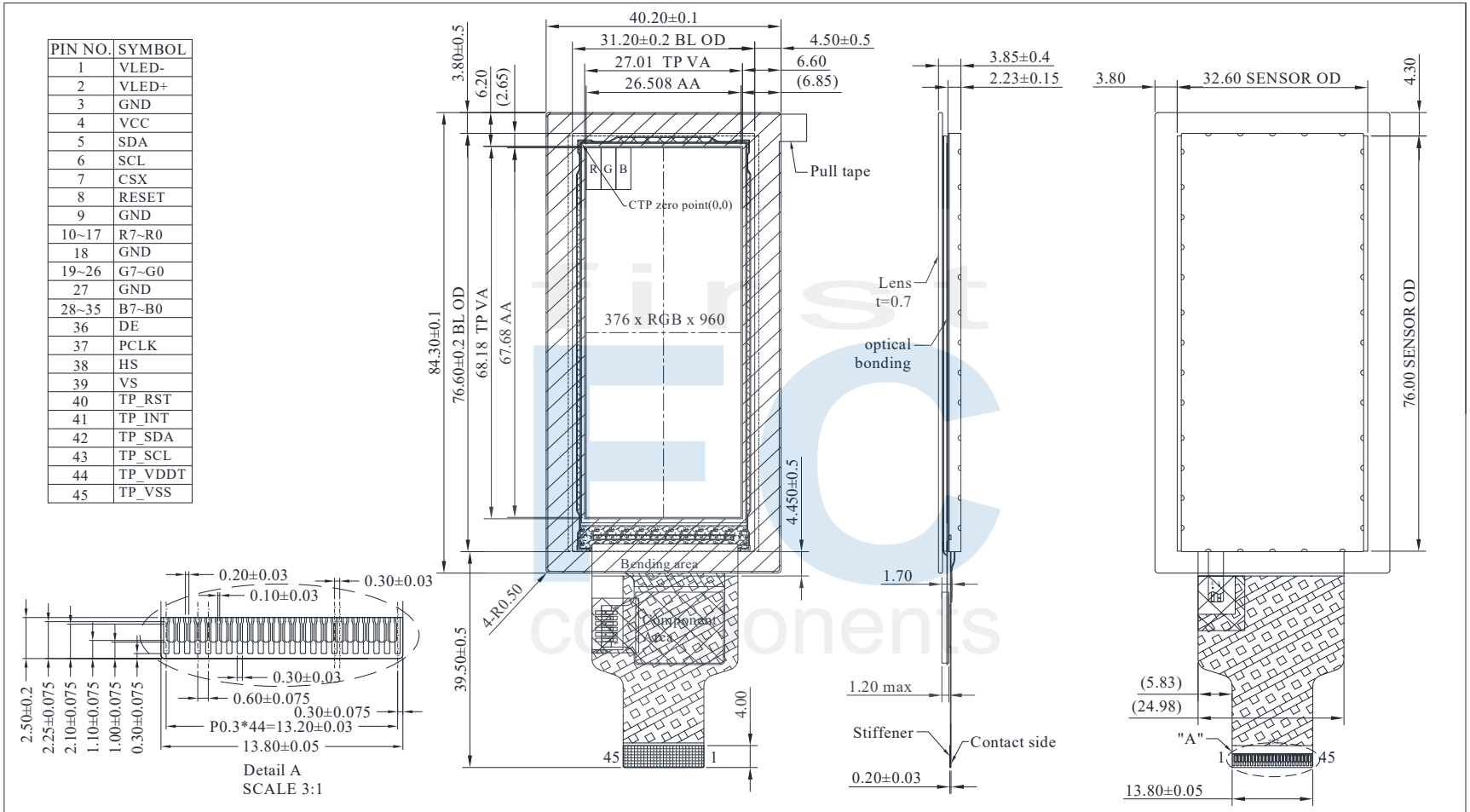
Match connector: Molex 5025984593 or equivalent.

Pin No.	Symbol	Description
1	VLED-	LED backlight cathode
2	VLED+	LED backlight anode
3	GND	Power ground
4	VCC	Power Supply for Digital Circuit
5	SDA	SDA: Serial data input/output bidirectional pin for SPI Interface.
6	SCL	SCL: Serial clock input for SPI interface.
7	CSX	- A chip select signal Low: the chip is selected and accessible High: the chip is not selected and not accessible
8	RESET	Reset signal(low active)
9	GND	Power ground
10~17	R7~R0	Red Data 7~0
18	GND	Power ground
19~26	G7~G0	Green Data 7~0
27	GND	Power ground
28~35	B7~B0	Blue Data 7~0
36	DE	Data Enable (ENABLE)
37	PCLK	Clock Signals ; Latch Data at the Falling Edge (DOTCLK)
38	HS	Line synchronizing signal for RGB interface operation (HSYNC)
39	VS	Frame synchronizing signal for RGB interface operation (VSYNC)
40	TP_RST	CTP External Reset, Low is active
41	TP_INT	CTP External interrupt to the host
42	TP_SDA	CTP I2C data input and output
43	TP_SCL	CTP I2C clock input
44	TP_VDDT	CTP Power supply: +3.3V
45	TP_VSS	CTP Ground for analog circuit

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Contour Drawing

PIN NO.	SYMBOL
1	VLED-
2	VLED+
3	GND
4	VCC
5	SDA
6	SCL
7	CSX
8	RESET
9	GND
10~17	R7~R0
18	GND
19~26	G7~G0
27	GND
28~35	B7~B0
36	DE
37	PCLK
38	HS
39	VS
40	TP_RST
41	TP_INT
42	TP_SDA
43	TP_SCL
44	TP_VDDT
45	TP_VSS



The non-specified tolerance of dimension is ±0.3 mm .

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