**Winstar Display Co., LTD**
**華凌光電股份有限公司**
*WEB: https://www.winstar.com.tw E-mail: sales@winstar.com.tw*

# SPECIFICATION

**CUSTOMER :** _____

**MODULE NO.:** WF70-800480A2D#A03-FC

| | |
|---|---|
| **APPROVED BY:**<br>**( FOR CUSTOMER USE ONLY )** | **PCB VERSION:** **DATA:** |

| SALES BY | APPROVED BY | CHECKED BY | PREPARED BY |
|---|---|---|---|
| | | | 葉虹蘭 |
| **ISSUED DATE:** 2021/04/14 | | | |

Represented by:

FIRST Components s.r.l.
www.first-components.com
technical@first-components.com
+39 0332 1888005

# 3.General Specifications

| Item | Dimension | Unit |
|---|---|---|
| Size | 7.0 | inch |
| Dot Matrix | 800 x RGB x 480 | dots |
| Module dimension | 165.0 x 100.0x 7.4 | mm |
| Active area | 154.08 x 85.92 | mm |
| Pixel Pitch | 0.1926 X 0.179 | mm |
| LCD type | TFT, Normally White, Transmissive | |
| View Direction | 12 o'clock | |
| Gray Scale Inversion Direction | 6 o'clock | |
| Aspect Ratio | 16:9 | |
| Backlight Type | LED ,Normally White | |
| TFT Interface | 24-bit RGB | |
| Color arrangement | RGB-STRIPE | |
| Driver IC | Source IC: ST-5623D, Gate IC: ST5091D or Equivalent | |
| CTP IC | ILI2130 or Equivalent | |
| CTP Interface | I2C | |
| CTP FW Version | 0x07.0x00.0x00.0x00.0x65.0x90.0x00.0x01 | |
| With /Without TP | With CTP | |
| Surface | Glare | |

*Color tone slight changed by temperature and driving voltage.

# 4.Absolute Maximum Ratings

| Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operating Temperature | TOP | -20 | — | +70 | ℃ |
| Storage Temperature | TST | -30 | — | +80 | ℃ |

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

1. Temp. ≦60℃, 90% RH MAX. Temp.＞60℃, Absolute humidity shall be less than 90% RH at 60℃

# 9.Interface

### 9.1. LCM PIN Definition

| Pin | Symbol | Function | Remark |
|---|---|---|---|
| 1 | A | Power supply for backlight | |
| 2 | A | Power supply for backlight | |
| 3 | K | Backlight ground | |
| 4 | K | Backlight ground | |
| 5 | GND | Power ground | |
| 6 | VCOM | Common voltage | |
| 7 | VCC | Power for Digital Circuit | |
| 8 | MODE | DE/SYNC mode select | Note 1 |
| 9 | DE | Data Input Enable | |
| 10 | VS | Vertical Sync Input | |
| 11 | HS | Horizontal Sync Input | |
| 12 | B7 | Blue data(MSB) | |
| 13 | B6 | Blue data | |
| 14 | B5 | Blue data | |
| 15 | B4 | Blue data | |
| 16 | B3 | Blue data | |
| 17 | B2 | Blue data | |
| 18 | B1 | Blue data | Note 2 |
| 19 | B0 | Blue data(LSB) | Note 2 |
| 20 | G7 | Green data(MSB) | |
| 21 | G6 | Green data | |
| 22 | G5 | Green data | |
| 23 | G4 | Green data | |
| 24 | G3 | Green data | |
| 25 | G2 | Green data | |
| 26 | G1 | Green data | Note 2 |
| 27 | G0 | Green data(LSB) | Note 2 |
| 28 | R7 | Red data(MSB) | |
| 29 | R6 | Red data | |
| 30 | R5 | Red data | |
| 31 | R4 | Red data | |
| 32 | R3 | Red data | |

| | | | |
|---|---|---|---|
| 33 | R2 | Red data | |
| 34 | R1 | Red data | Note 2 |
| 35 | R0 | Red data(LSB) | Note 2 |
| 36 | GND | Power Ground | |
| 37 | DCLK | Sample clock (CLK) | Note 3 |
| 38 | GND | Power Ground | |
| 39 | L/R | Left / right selection | Note 4 |
| 40 | U/D | Up/down selection | Note 5 |
| 41 | VGH | Gate ON Voltage | |
| 42 | VGL | Gate OFF Voltage | |
| 43 | AVDD | Power for Analog Circuit | |
| 44 | RESET | Global reset pin. | Note 6 |
| 45 | NC | No connection | |
| 46 | VCOM | Common Voltage | |
| 47 | DITHB | Dithering function | Note 7 |
| 48 | GND | Power Ground | |
| 49 | NC | No connection | |
| 50 | NC | No connection | |

I: input, O: output, P: Power

Note 1: When select DE mode, MODE="1", VS and HS must pull high.
When select SYNC mode, MODE= "0", DE must be grounded.

Note 2: When input 18 bits RGB data, the two low bits of R,G and B data must be grounded.

Note 3: Data shall be latched at the falling edge of DCLK.

Note 4: Source Right or Left sequence control
L/R="L", shift left: last data=S1←S2←S3…←S1200=first data
L/R="H", shift left: last data=S1←S2←S3…←S1200=last data

Note 5: Gate Up or Down scan control
U/D="L", STV2 output vertical start pulse and UD pin output logical "0" to gate driver
U/D="H", STV1 output vertical start pulse and UD pin output logical "1" to gate driver

Note 6: Global reset pin. Active low to enter reset state . Suggest to connect with an RC reset circuit for stability. Normally pull high.

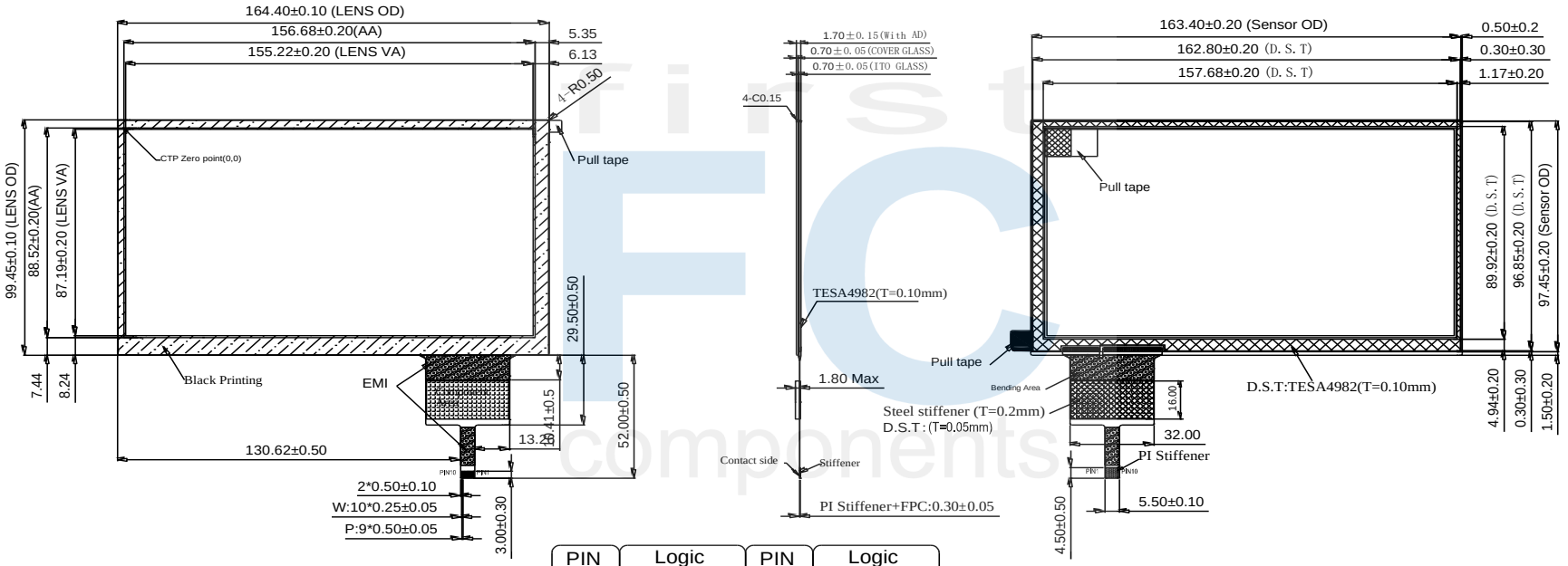
Note 7: Dithering function enable control, normally pull high.
When DITHB="1", Disable internal dithering function,
When DITHB="0", Enable internal dithering function,

### 9.2. CTP PIN Definition

| Pin | Symbol | Function | Remark |
|---|---|---|---|
| 1 | VSS | Ground for analog circuit | |
| 2 | VDDT | Power Supply : +3.3V | |
| 3 | SCL | I2C clock input | |
| 4 | NC | No connect | |
| 5 | SDA | I2C data input and output | |
| 6 | NC | No connect | |
| 7 | RST | External Reset, Low is active | |
| 8 | NC | No connect | |
| 9 | INT | External interrupt to the host | |
| 10 | VSS | Ground for analog circuit | |

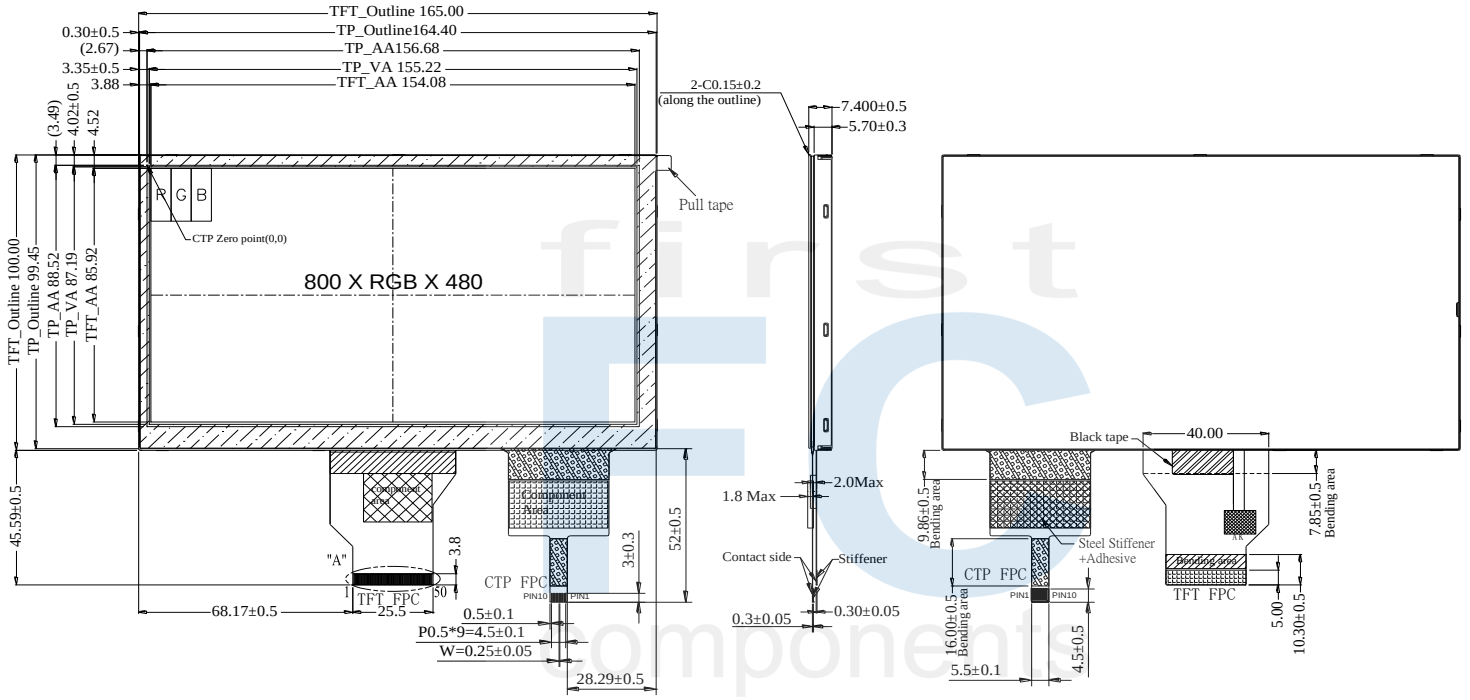
first FC components

# 12.Touch Panel Information




| PIN | Logic | PIN | Logic |
|---|---|---|---|
| 1 | VSS | 6 | NC |
| 2 | VDDT | 7 | /RST |
| 3 | SCL | 8 | NC |
| 4 | NC | 9 | /INT |
| 5 | SDA | 10 | VSS |

# 13.Contour Drawing




TFT FPC

| PIN | |
|---|---|
| 1 | A |
| 2 | A |
| 3 | K |
| 4 | K |
| 5 | GND |
| 6 | VCOM |
| 7 | VCC |
| 8 | MODE |
| 9 | DE |
| 10 | VS |
| 11 | HS |
| 12 | B7 |
| 13 | B6 |
| 14 | B5 |
| 15 | B4 |
| 16 | B3 |
| 17 | B2 |
| 18 | B1 |
| 19 | B0 |
| 20 | G7 |
| 21 | G6 |
| 22 | G5 |
| 23 | G4 |
| 24 | G3 |
| 25 | G2 |
| 26 | G1 |
| 27 | G0 |
| 28 | R7 |
| 29 | R6 |
| 30 | R5 |
| 31 | R4 |
| 32 | R3 |
| 33 | R2 |
| 34 | R1 |
| 35 | R0 |
| 36 | GND |
| 37 | DCLK |
| 38 | GND |
| 39 | L/R |
| 40 | U/D |
| 41 | VGH |
| 42 | VGL |
| 43 | AVDD |
| 44 | RESET |
| 45 | NC |
| 46 | VCOM |
| 47 | DITHB |
| 48 | GND |
| 49 | NC |
| 50 | NC |

CTP FPC

| PIN | |
|---|---|
| 1 | VSS |
| 2 | VDDT |
| 3 | SCL |
| 4 | NC |
| 5 | SDA |
| 6 | NC |
| 7 | RST |
| 8 | NC |
| 9 | INT |
| 10 | VSS |

A:SCALE:5X

The non-specified tolerance of dimension is ±0.3 mm .