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SPECIFICATION

CUSTOMER : _____

MODULE NO.: WF35CTIACDA#

APPROVED BY: **(FOR CUSTOMER USE ONLY)**	**PCB VERSION:** **DATA:**

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY
first FC components			
ISSUED DATE:			

2.SUMMARY

This technical specification applies to 3.45 “ color TFT-LCD panel. The 3.45 “ color TFT-LCD panel is designed for camcorder, digital camera application and other electronic products which require high quality flat panel displays. This module follows RoHS.

FEATURES

High Resolution :230,400 Dots (320 RGB x 240) . Image Reversion: Up/Down and Left/Right.

3.General Specification

Item	Dimension	Unit
Dot Matrix	320 x RGBx240(TFT)	dots
Module dimension	76.9 x 63.9 x 3.3	mm
Active area	70.08 x 52.56	mm
Dot pitch	0.073 x 0.219	mm
LCD type	TFT, Negative, Transmissive	
View direction	6 o’clock	
Backlight Type	LED,Normally White	

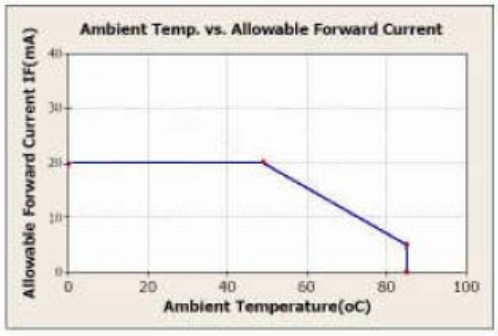
*Color tone slight changed by temperature and driving voltage.

4.Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_{OP}	-20	—	+70	℃
Storage Temperature	T_{ST}	-30	—	+80	℃
Power Supply Voltage	DVDD,AVDD	-0.3	—	5.0	V
Input signal voltage	V_{IN}	-0.3	—	VDD+0.3	V
Logic output voltage	V_{OUT}	-0.3	—	VDD+0.3	

Note: Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above

1. Temp. ≦60^0C, 90% RH MAX. Temp. ＞ 60^0C , Absolute humidity shall be less than 90% RH at 60^0C



9. INTERFACE

9.1. LCM PIN Definition

Pin	Symbol	I/O	Function	Remark
1	VBL-	I	Backlight LED Ground	
2	VBL-	I	Backlight LED Ground	
3	VBL+	I	Backlight LED Power	
4	VBL+	I	Backlight LED Power	
5	Y1	I	Top electrode	
6	X1	I	Right electrode	
7	NC		Not use	
8	/RESET	-	Hardware reset	
9	SPENA	I	SPI interface Data Enable signal	
10	SPCLK	I	SPI interface Data Clock	
11	SPDAT	I	SPI interface Data	
12	B0	I	Blue Data Bit 0	
13	B1	I	Blue Data Bit 1	
14	B2	I	Blue Data Bit 2	
15	B3	I	Blue Data Bit 3	
16	B4	I	Blue Data Bit 4	
17	B5	I	Blue Data Bit 5	
18	B6	I	Blue Data Bit 6	
19	B7	I	Blue Data Bit 7	
20	G0	I	Green Data Bit 0	
21	G 1	I	Green Data Bit 1	
22	G 2	I	Green Data Bit 2	
23	G 3	I	Green Data Bit 3	
24	G 4	I	Green Data Bit 4	
25	G 5	I	Green Data Bit 5	
26	G 6	I	Green Data Bit 6	
27	G 7	I	Green Data Bit 7	
28	R0	I	Red Data Bit0/DX0	
29	R1	I	Red Data Bit1/DX1	
30	R2	I	Red Data Bit2/DX2	
31	R3	I	Red Data Bit3/DX3	
32	R4	I	Red Data Bit4/DX4	
33	R5	I	Red Data Bit5/DX5	
34	R6	I	Red Data Bit6/DX6	
35	R7	I	Red Data Bit7/DX7	
36	HSYNC	I	Horizontal sync input	
37	VSYNC	I	Vertical sync input	
38	DCLK	I	Dot Data Clock	
39	NC		Not use	
40	NC		Not use	
41	Vcc	I	Digital power	
42	Vcc	I	Digital power	
43	Y2	I	Bottom electrode	
44	X2	I	Left electrode	
45	NC		Not use	
46	NC		Not use	
47	NC		Not use	
48	IF2	I	Control the input data format /floating	

49	IF1	I	Control the input data format	
50	IF0	I	Control the input data format	
51	NC		Not use	
52	DE	I	Data Enable input	
53	GND	I	Ground	
54	GND	I	Ground	

Note:

1. The mode control (IF2) not use, it can't control CCIR601 interface, If not use CCIR601, it can floating.
2. For digital RGB input data format, both SYNC mode and DE+SYNC mode are supported. If DE signal is fixed low, SYNC mode is used. Otherwise, DE+SYNC mode is used. Suggest used SYNC mode!!_
3. Usually pull high._
4. IF select serial RGB or CCIR601/656 input mode is selected, only DX0-DX7 used, and the other short to GND, Only selected serial RGB_CCIR601/656 interface, DX BUS will enable, Digital input mode DX0 is LSB and DX7 is MSB.
5. Control the input data format.

IF2-0: Define the input interface mode.

IF2	IF1	IF0	Format	Operating Frequency
0	0	0	Parallel-RGB data format (only support stripe type color filter)	6.5MHz
0	0	1	Serial-RGB data format	19.5MHz
0	1	0	CCIR 656 data format (640RGB)	24.54MHz
0	1	1	CCIR 656 data format (720RGB)	27MHz
1	0	0	YUV mode A data format (Cr-Y-Cb-Y)	24.54MHz
1	0	1	YUV mode A data format (Cr-Y-Cb-Y)	27MHz
1	1	0	YUV mode B data format (Cb-Y-Cr-Y)	27MHz
1	1	1	YUV mode B data format (Cb-Y-Cr-Y)	24.54MHz

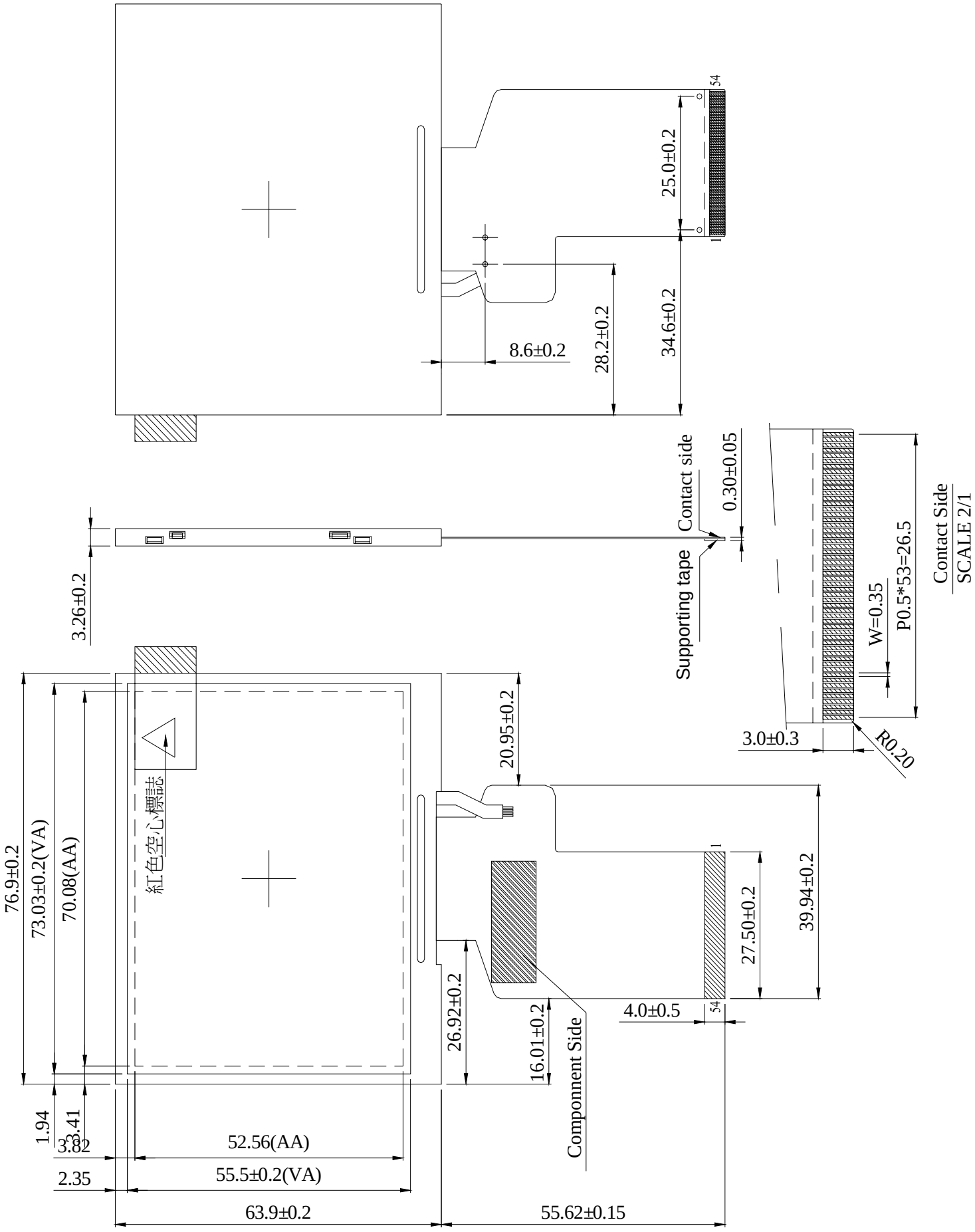
Input format	DOTCLK Freq (MHz)	Display Data	Active Area (DOTCLK)
YUV mode	24.54	640	1280
	27	720	1440

Mode	D[23:16]	D[15:8]	D[7:0]	IHS	IVS	DEN
ITU-R BT 656	D[23:16]	GND	GND	NC	NC	NC
ITU-R BT 601	D[23:16]	GND	GND	IHS	IVS	NC
8 bit RGB	D[23:16]	GND	GND	IHS	IVS	NC for HV Mode DEN for DEN Mode
24 bit RGB	R[7:0]	G[7:0]	B[7:0]	IHS	IVS	NC for HV Mode DEN for DEN Mode

9.2 SPI timing Characteristics

PARAMETER	Symbol	Min.	Typ.	Max.	Unit
SPCK period	T_{CK}	60	-	-	ns
SPCK high width	T_{CKH}	30	-	-	ns
SPCK low width	T_{CKL}	30	-	-	ns
Data setup time	T_{SU1}	12	-	-	ns
Data hold time	T_{HD1}	12	-	-	ns
SPENA to SPCK setup time	T_{CS}	20	-	-	ns
SPENA to SPDA hold time	T_{CS}	20	-	-	ns
SPENA high pulse width	T_{CD}	50	-	-	ns
SPDA output latency	T_{CS}	-	1/2	-	T_{CK}

12.Contour Drawing



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web: www.first-components.com

PIN NO.	SYMBOL	PIN NO.	SYMBOL	PIN NO.	SYMBOL
1	VBL-	21	G1	41	VCC
2	VBL-	22	G2	42	VCC
3	VBL+	23	G3	43	Y2
4	VBL+	24	G4	44	X2
5	Y1	25	G5	45	NC
6	X1	26	G6	46	NC
7	NC	27	G7	47	NC
8	/RESET	28	R0	48	IF2
9	SPENA	29	R1	49	IF1
10	SPCLK	30	R2	50	IF0
11	SPDAT	31	R3	51	NC
12	B0	32	R4	52	DE
13	B1	33	R5	53	GND
14	B2	34	R6	54	GND
15	B3	35	R7		
16	B4	36	Hsync		
17	B5	37	Vsync		
18	B6	38	DATA CLK		
19	B7	39	NC		
20	G0	40	NC		