VGG243271-6UFLWA-FC

GENERAL SPECIFICATION

ITEM	CONTENTS
Module Size	42.72 (W) * 91.16 (H) * 2.8 (T) mm
Display Size	2.4 inch
Display Format	240(RGB)* 320 Pixels
Active Area	36.72 (W) * 48.96 (H) mm
Pixel Pitch	0.153 * 0.153 mm
LCD Type	TFT (262K)/ Transmissive / Positive
View Angle	6 O'clock (The Gray Inversion will appear at this direction)
Controller IC	ILI9325
Backlight Driver type	External Power
DC to DC circuit	Build-In
Approx. Weight	13.3g

ABSOLUTE MAXIMUM RATING(Ta=25℃ VSS=0V)

Item	Symbol	Min.	Type	Max.	Unit	Humidity
Supply Voltage	V_{CC}-V_{SS}	-0.3	-	+4.0	Volt	-
Operating Temperature	Top	-20	-	+70	℃	Note1
Storage Temperature	Tst	-30	-	+80	℃	Note2

Note1: Background color changes slightly depending on ambient temperature. This phenomenon is reversible.

Ta≦70℃: 75%RH max

Ta>70℃: absolute humidity must be lower than the humidity of 75%RH at 70℃

Note2: Ta at -30℃ will be <48hrs, at 80 ℃ will be <120hrs

ELECTRO-OPTICAL CHARACTERISTICS (Ta＝25℃)

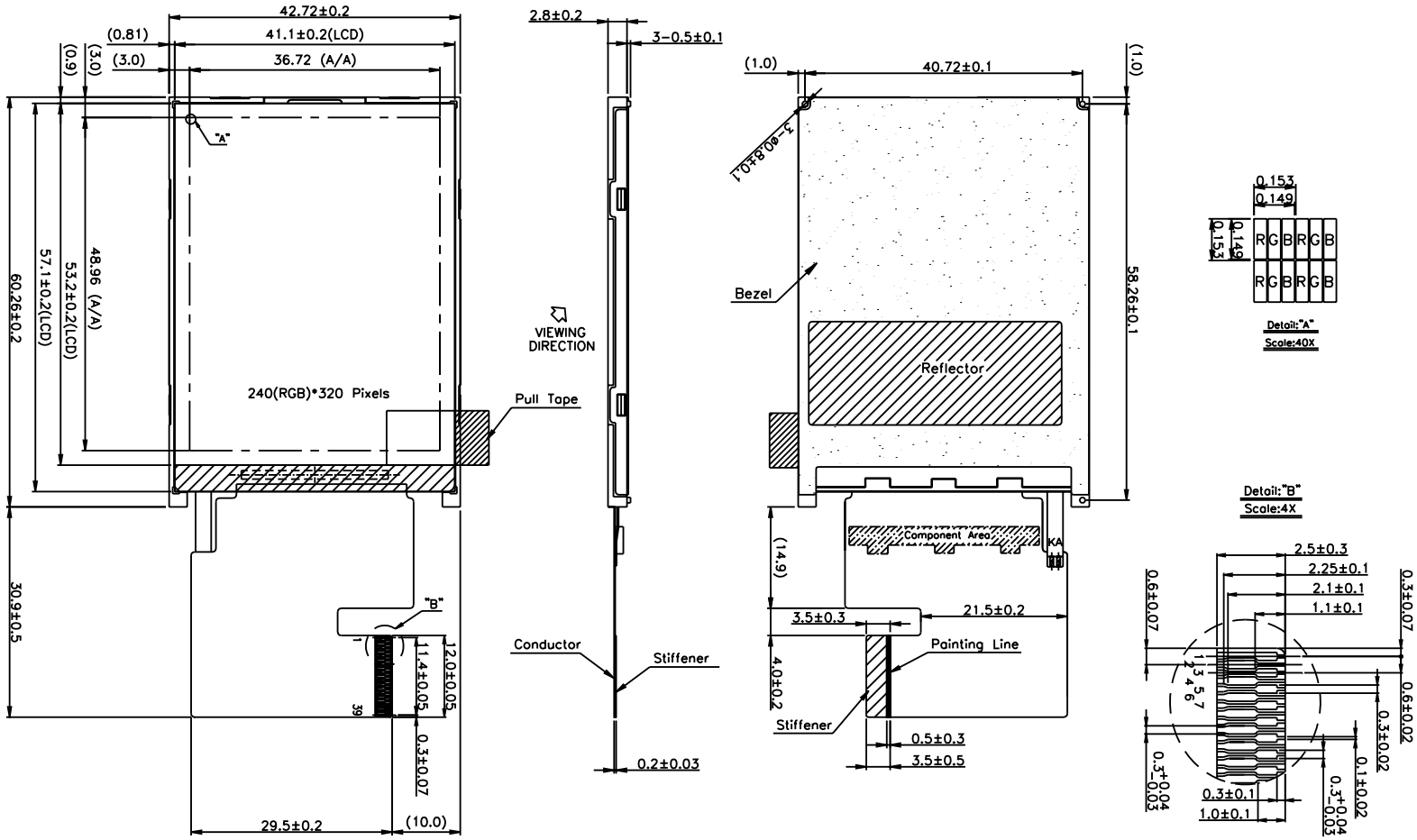
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply for Logic	IOVCC	-	-	2.8	-	Volt
Power Supply Current for LCM	I_{DD}	IOVCC=2.8V	-	5.6	7.9	mA
Current consumption during sleeping mode	I_{ST}	IOVCC=2.8V Ta=25℃	-	100	200	uA

INTERFACE PIN ASSIGNMENT

<table>
<tr><th>No.</th><th>Symbol</th><th>Function</th></tr>
<tr><td>1
2
3</td><td>IM0
IM1
IM2</td><td>Select the MPU system interface mode.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU-Interface</th><th>DB Pin in use</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting invalid</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Setting invalid</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>I80-system 16-bit interface</td><td>DB[17:10],DB[8:1]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>I80-system 8-bit interface</td><td>DB[17:10]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ID</td><td>Serial Peripheral interface(SPI)</td><td>SDI,SDO</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>*</td><td>Setting invalid</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Setting invalid</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Setting invalid</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>I80-system 18-bit interface</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>I80-system 9-bit interface</td><td>DB[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>*</td><td>*</td><td>Setting invalid</td><td>-</td></tr>
</table></td></tr>
<tr><td>4</td><td>IM3</td><td>When the serial peripheral interface is selected,IM0 pin is used for the device code ID setting.</td></tr>
<tr><td>5</td><td>nRESET</td><td>A reset pin.
Initializes the ILI9325 with a low input. Be sure to execute a power-on reset after supplying power.</td></tr>
<tr><td>6</td><td>VSYNC</td><td>Frame synchronizing signal for RGB interface operation.
VSPL="0":Active low
VSPL="1"Active high
Fix to GND level when not in use.</td></tr>
<tr><td>7</td><td>HSYNC</td><td>Line synchronizing signal for RGB interface operation.
HSPL="0"=Active low
HSPL="1":Active high
Fix to GND level when not in use.</td></tr>
<tr><td>8</td><td>DOTCLK</td><td>Dot clock signal for RGB interface operation.
DPL = "0": Input data on the rising edge of DOTCLK
DPL = "1": Input data on the falling edge of DOTCLK
Fix to GND level when not in use.</td></tr>
<tr><td>9</td><td>ENABLE</td><td>Data ENEABLE signal for RGB interface operation.
Low: Select (access enabled)
High: Not select (access inhibited)
The EPL bit inverts the polarity of the ENABLE signal.
Fix to either IOVcc or GND level when not in use.</td></tr>
</table>

No.	Symbol	Function
10 ~ 27	DB17~DB0	An 18-bit parallel bi-directional data bus for MPU system interface mode. 8-bit I/F: DB [17:10] is used. 9-bit I/F: DB [17:9] is used. 16-bit I/F: DB [17:10] and DB [8:1] is used. 18-bit I/F: DB [17:0] is used. 18-bit parallel bi-directional data bus for RGB interface operation. 6-bit RGB I/F: DB [17:12] are used. 16-bit RGB I/F: DB[17:13] and DB[11:1] are used. 18-bit RGB I/F: DB[17:0] are used. Unused pins must be fixed GND level.
28	SDO	SPI interface output pin. The data is outputted on the falling edge of the SCL signal. Let SDO as floating when not used.
29	SDI	SPI interface input pin. The data is latched on the rising edge of the SCL signal.
30	nRD	A read strobe signal and enables an operation to read out data when the signal is low. Fix to either IOVcc or GND level when not in use.
31	nWR/SCL	A write strobe signal and enables an operation to write data when the signal is low. Fix to either IOVcc or GND level when not in use. SPI Mode: Synchronizing clock signal in SPI mode.
32	RS	A register select signal. Low: select an index or status register High: select a control register Fix to either IOVcc or GND level when not in use.
33	nCS	A chip select signal. Low: the ILI9325 is selected and accessible High: the ILI9325 is not selected and not accessible Fix to the GND level when not in use.
34	GND	Ground
35	IOVCC	Power supply voltage.
36~37	GND	Ground

No.	Symbol	Function
38	LED-	LED Cathode
39	LED+	LED Anode


42.72±0.2
(0.81)
41.1±0.2(LCD)
(0.9)
(3.0)
36.72 (A/A)
"A"
60.26±0.2
57.1±0.2(LCD)
53.2±0.2(LCD)
48.96 (A/A)
240(RGB)*320 Pixels
Pull Tape
30.9±0.5
"B"
11.4±0.05
12.0±0.05
39
0.3±0.07
29.5±0.2
(10.0)
2.8±0.2
3-0.5±0.1
VIEWING DIRECTION
Conductor
Stiffener
0.2±0.03
(1.0)
40.72±0.1
(1.0)
3-0.8±0.1
Bezel
58.26±0.1
Reflector
(14.9)
Component Area
KA
3.5±0.3
21.5±0.2
Painting Line
4.0±0.2
Stiffener
0.5±0.3
3.5±0.5
0.153
0.149
0.149
0.153
R G B R G B
R G B R G B
Detail:"A"
Scale:40X
Detail:"B"
Scale:4X
2.5±0.3
2.25±0.1
2.1±0.1
1.1±0.1
0.6±0.07
0.3±0.07
1 2 3 4 5 6 7
0.6±0.02
0.3±0.02
0.1±0.02
0.3±0.1
1.0±0.1
0.3+0.04 -0.03
0.3+0.04 -0.03