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ILI9881C-0D

Amorphous TFT LCD Single-Chip Driver 800(RGB) x 1280 Resolution, 16.7M-color Without Internal GRAM

first FC components

Specification

Version: V102
Document No: ILI9881C-0D_DTS_V102_20170316_Normal

ILI TECHNOLOGY CORP.
8F, No. 38, Taiyuan St, Jhubei City,
Taiwan 302, R.O.C.
Tel.886-3-5600099; Fax.886-3-5600585
http://www.ilitek.com

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1. Introduction

The ILI9881C-0D is a 16.7M single-chip (SOC) driver. It is comprised of a 2404-channel source driver (S1~S2400 and SDUM[3:0]), a gate-IC-less level shifter and a power supply circuit to drive a dot-matrix TFT LCD with 800 (RGB) x 1280 dots at maximum.

The ILI9881C-0D can configure functions via the MIPI[1] DSI[2] Interface; transmit video data via MIPI DSI Interface. The ILI9881C-0D supports three kinds of data types, i.e., 16-bit, 18-bit and 24-bit, for video image display in MIPI DSI interfaces. In the MIPI DSI high-speed mode, the ILI9881C-0D also provides three user-selectable hardware structures:

- Two data lane supports up to 850Mbps on the MIPI DSI link
- Three data lanes support up to 700Mbps on the MIPI DSI link
- Four data lanes support up to 550Mbps on the MIPI DSI link

The ILI9881C-0D can operate with 1.65V I/O interface voltage and supports a wide range of analog power supplies. The ILI9881C-0D supports 2 colors (Idle Mode: 2-color low power mode) display and sleep mode power management functions, ideal for portable products where battery power conservation is desirable, such as digital cellular phones, smart phones, MP3 players, personal media players and similar devices with color graphics displays.

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[1] *MIPI: Mobile Industry Processor Interface*

[2] *DSI: Display Serial Interface*

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2. Features

- Display resolution options:
  - 800 (RGB) (H) x (480 + (4 x NL) (V)
  - 768 (RGB) (H) x (480 + (4 x NL) (V)
  - 720 (RGB) (H) x (480 + (4 x NL) (V)

- Display color modes
  - Full color mode:

    16.7M colors (24-bit data, R: 8-bit, G: 8-bit, B: 8-bit)
  - Reduced color modes:

    262K colors (18-bit data, R: 6-bit, G: 6-bit, B: 6-bit)

    65K colors (16-bit data, R: 5-bit, G: 6-bit, B: 5-bit)

    2 colors (Idle Mode: 2-color low power mode)

- Display module:
  - Supports 2404 source channel outputs (S1~S2400 and SDUM[3:0])
  - Supports gate control signals to gate driver in the panel
  - Supports 1-dot , 2-dot , 4-dot , N/4-dot , N/8-dot , N/16-dot , N/32-dot , column , Zig-Zag inversion
  - Gamma correction (1 preset Gamma curve)
  - On module VCOM control
  - 800x1280-dot display RAM with data compression for 2-color low power mode

- Display interface types:
  - DSI interface (DSI version 1.01 and D-PHY version 1.00):

    2 data lane / maximum speed 850Mbps

    3 data lanes / maximum speed 700Mbps

    4 data lanes / maximum speed 550Mbps

- Power saving modes:
  - Sleep mode

- Other on-chip functions/Miscellaneous
  - Software programmable color depth mode
  - Oscillator for display clock generation
  - DC VCOM voltage generator and adjustment
  - CABC (Content Adaptive Brightness Control) function
  - DGC (Digital Gamma Correction) function
  - IIE (Impressive Image Enhancement) function
  - VGH/VGL voltage generator for gate control signal in panel
  - Gate control signals to gate driver in panel (GIP)
  - OTP (One-Time Programming) memory store initialization register settings
  - Provide 3 times to store DC VCOM value setting and ID1 ~ ID3
  - BIST (Built-In Self-Test Pattern) mode function

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- Input power:
  - VCI = 2.5V ~ 6.6V
  - VDDI = 1.65V ~ 3.6V
  - VCC1 = 1.65V ~ 6.6V
  - VCC2 = 1.65V ~ 6.6V
  - VDDAM = 1.65V ~ 3.6V
  - VSP = 4.5V ~ 6.6V
  - VSN = -6.6V ~ -4.5V
  - OTP programming voltage (MTP_PWR): 8.5V

- Source/VCOM/Gate power supply voltage:
  - VCL-GND = -3.0V ~ -2.3V
  - DC VCOM = -4.0V ~ -0.2V (12mV/step); 0V
  - VREG1OUT = 3.5V ~ 5.6V (Positive source output voltage level)
  - VREG2OUT = -5.6V ~ -3.5V (Negative source output voltage level)
  - VGH-GND = 8V ~ 18V (Positive gate driver output voltage level)
  - VGL-GND = -7V ~ -18V (Negative gate driver output voltage level)

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3. Device Overview

3.1. Block Diagram

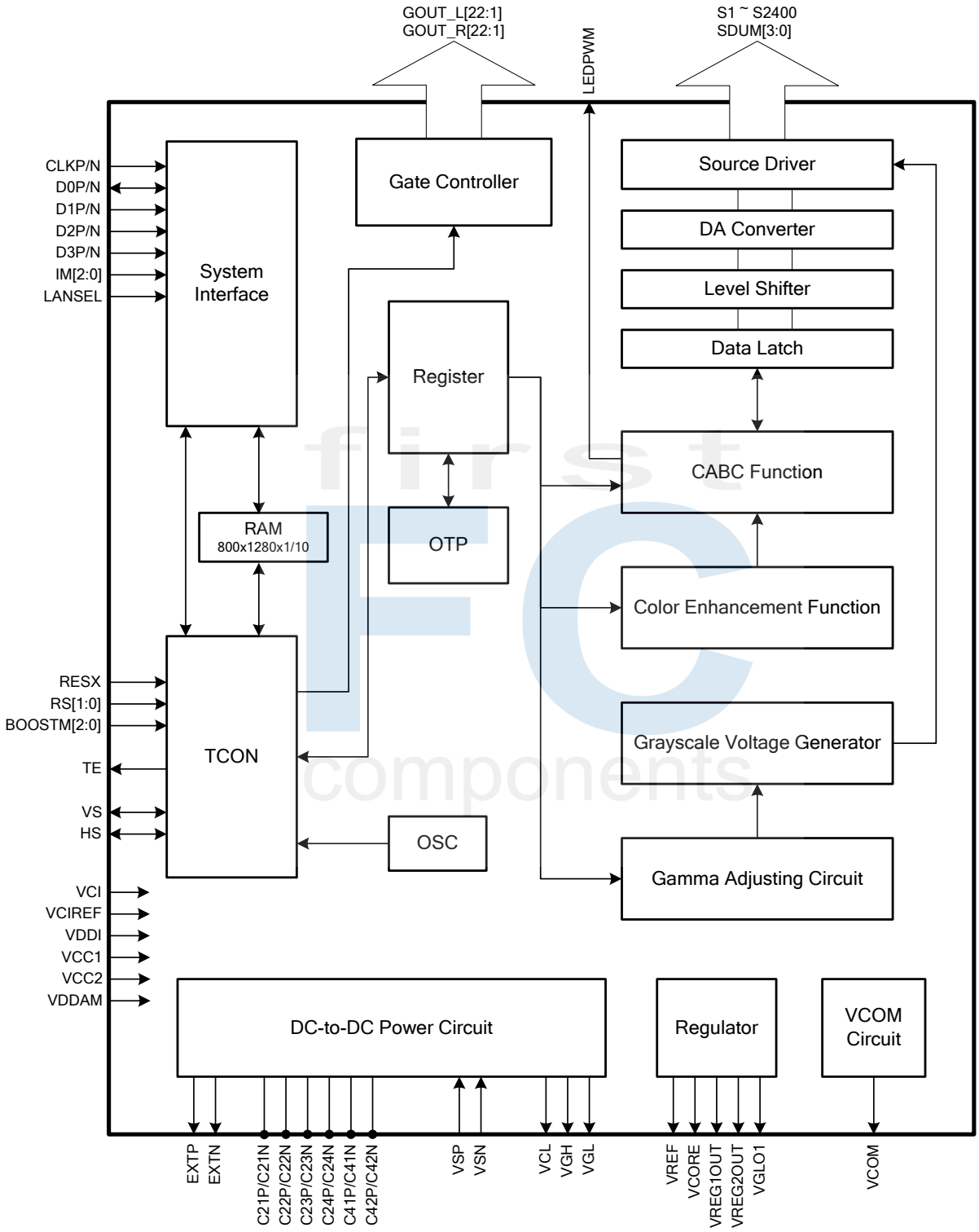


Figure 1: Block Diagram

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3.2. Block Function Description

3.2.1. System Interface

The ILI9881C-0D supports DSI interfaces. The interface mode and the lane number of DSI interface can be selected by hardware pins IM[2:0], LANSEL and control register MIPI_LANE_SEL (Page4_R00h).

3.2.2. Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates a liquid crystal drive voltage that corresponds to the grayscale level set in the Gamma correction register. The ILI9881C-0D can display 16.7M colors at maximum.

3.2.3. TCON

The TCON generates timing signals for internal circuits. Timing for display operations are outputted separately so that they do not interfere with each other.

3.2.4. OSC

The ILI9881C-0D incorporates with an RC oscillator circuit. Command settings are used to change the frame frequency.

3.2.5. RAM

The LCD driver incorporates the RAM (800x1280)/10 bits = 12800 bytes, which can store pattern data of a 800(RGB) x 1280 resolution with data compression in the Idle Mode.

3.2.6. Source Driver Circuit

The LCD display driver circuit consists of a 2404-output source driver (S1~S2400 and SDUM[3:0]). The display pattern data is latched when 800RGB pixels of data are input. The voltage is output from the source driver according to the latched data.

3.2.7. Gate Controller Circuit

The panel control circuit outputs GOUT_L/R[22:1] signals at either the VGH or VGL level.

3.2.8. DC-to-DC Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels for driving a panel. Voltage levels are adjusted according to the register setting.

3.2.9. CABC (Content Adaptive Brightness Control)

The CABC (Content Adaptive Brightness Control) dynamic backlight control function is used to reduce the power consumption of the luminance source.

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3.3. Pin Descriptions

Table 1: Pin Definition

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Type</th><th>Descriptions</th></tr>
<tr><td colspan="4">Global Control Pins</td></tr>
<tr><td>IM[2:0]</td><td>I</td><td>VDDI</td><td>- Interface mode select pins.
Notes:
(1) IM[2:0] pins are used to configure lane sequence and polarity
(2) The bottom table is an example for MIPI 4 lane setting
<table>
<tr><th colspan="3">External Pad Set</th><th colspan="5">Configuration of MIPI Lane</th></tr>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>D0P/N Pin</th><th>D1P/N Pin</th><th>CLKP/N Pin</th><th>D2P/N Pin</th><th>D3P/N Pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>D3P/N</td><td>D2P/N</td><td>CLKP/N</td><td>D1P/N</td><td>D0P/N</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>D3N/P</td><td>D2N/P</td><td>CLKN/P</td><td>D1N/P</td><td>D0N/P</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>D0P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D2P/N</td><td>D3P/N</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>D0N/P</td><td>D1N/P</td><td>CLKN/P</td><td>D2N/P</td><td>D3N/P</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>D3P/N</td><td>D0P/N</td><td>CLKP/N</td><td>D1P/N</td><td>D2P/N</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>D3N/P</td><td>D0N/P</td><td>CLKN/P</td><td>D1N/P</td><td>D2N/P</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>D2P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D0P/N</td><td>D3P/N</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>D2N/P</td><td>D1N/P</td><td>CLKN/P</td><td>D0N/P</td><td>D3N/P</td></tr>
</table></td></tr>
<tr><td>RS[1:0]</td><td>I</td><td>VDDI</td><td>- Resolution selection pins.
<table>
<tr><th>RS1</th><th>RS0</th><th>Resolution</th></tr>
<tr><td>0</td><td>0</td><td>800 (RGB) x (480 + (4 x NL)) gate line</td></tr>
<tr><td>0</td><td>1</td><td>768 (RGB) x (480 + (4 x NL)) gate line</td></tr>
<tr><td>1</td><td>0</td><td>720 (RGB) x (480 + (4 x NL)) gate line</td></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>LANSEL</td><td>I</td><td>VDDI</td><td>- MIPI DSI Lane number selection pin
LANSEL=”1”, MIPI DSI is 2 Lane mode
LANSEL=”0”, MIPI DSI is 3 or 4 Lane mode
Note: Please reference “Table 2 DSI Interface Lane Mode Selection”</td></tr>
<tr><td>BOOSTM[2:0]</td><td>I</td><td>VDDI</td><td>- Power type selection pins
<table>
<tr><th>Page4_R6Eh
DI_PWR_REG</th><th>BOOSTM2</th><th>BOOSTM1</th><th>BOOSTM0</th><th>NOTE</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Power Mode 2A
External VDDI, VSP and VSN (VCI=VSP)
Note 1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Power Mode 4
External VDDI, VCI, VSP and VSN</td></tr>
<tr><td>X</td><td>0</td><td>1</td><td>0</td><td>Power Mode 3
External VDDI and VCI (with ILI4003)</td></tr>
<tr><td colspan="4">prohibited</td><td>-</td></tr>
</table>
The default value of DI_PWR_REG is “1”.
Note 1: VCI and VSP pads must be connected by external metal path.</td></tr>
<tr><td>RESX</td><td>I</td><td>VDDI</td><td>- The external reset input
Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.
Fix to VDDI level when not in use.</td></tr>
<tr><td>TE</td><td>O</td><td>VDDI</td><td>- Tearing effect output pin.
Leave the pin open when not in use.</td></tr>
<tr><td>VS</td><td>I/O</td><td>VDDI</td><td>- Touch synchronization signal (VSOUT).
Fix to VSS level when not in use.</td></tr>
<tr><td>HS</td><td>I/O</td><td>VDDI</td><td>- Touch synchronization signal (HSOUT).
Fix to VSS level when not in use.</td></tr>
<tr><td>LEDPWM</td><td>O</td><td>VDDI</td><td>- LCD backlight control PWM output pin.
Leave the pin open when not in use.</td></tr>
<tr><td colspan="4">DSI Interface Signal Pins</td></tr>
<tr><td>CLKP
CLKN</td><td>I</td><td>LVDSVDD</td><td>- MIPI DSI differential clock pair
Leave it open or fix to LVDSVSS level when not in use.</td></tr>
<tr><td>D0P
D0N</td><td>I/O</td><td>LVDSVDD</td><td>- MIPI DSI differential data pair. (Data lane 0)
Leave it open or fix to LVDSVSS level when not in use.</td></tr>
</table>

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D1P D1N	I	LVDSVDD	- MIPI DSI differential data pair. (Data lane 1) Leave it open or fix to LVDSVSS level when not in use.
D2P D2N	I	LVDSVDD	- MIPI DSI differential data pair. (Data lane 2) Leave it open or fix to LVDSVSS level when not in use.
D3P D3N	I	LVDSVDD	- MIPI DSI differential data pair. (Data lane 3) Leave it open or fix to LVDSVSS level when not in use.
Source / Panel Control / VCOM Signal Pins			
S[2400:1]	O	Analog	- Output source driver signals. The D/A converted 256-gray-scale analog voltage output. Source output mapping with different resolution Disaply resulation / Source channels 800 (RGB) / S1 ~ S2400 768 (RGB) / S1 ~ S1152, S1249 ~ S2400 720 (RGB) / S1 ~ S1080, S1321 ~ S2400 800 (RGB) + Zig-Zag / S1 ~ S2400, SDUM[2:1]
SDUM[3:0]	O	Analog	- Dummy Source Leave the pin open when not in use.
GOUT_L[22:1]	O	Analog	- Gate control signals for panel in left side of IC Leave the pin open when not in use.
GOUT_R[22:1]	O	Analog	- Gate control signals for panel in right side of IC Leave the pin open when not in use.
VCOM	O	Analog	- Regulator output for common voltage of panel Connect to a stabilizing capacitor between VCOM and VSSA.
Power Supply Pins			
VCI	I	Power Supply	- Power supply for analog circuits. Connect to an external power supply of 2.5V to 6.6V
VCIREF	I	Power Supply	- Power supply for analog circuits. Connect to an external power supply of 2.5V to 6.6V
VDDI	I	Power Supply	- Power supply for I/O pads. Connect to an external power supply of 1.65V to 3.6V
VCC1	I	Power Supply	- Power supply for internal logic regulator. Connect to an external power supply of 1.65V to 6.6V
VCC2	I	Power Supply	- Power supply for internal logic regulator. Connect to an external power supply of 1.65V to 6.6V
VDDAM	I	Power Supply	- Power supply for MIPI DSI regulator. Connect to an external power supply of 1.65V to 3.6V
VSP	I	Power Supply	- Input voltage from step-up circuit. Connect to an external power supply of 4.5V to 6.6V
VSN	I	Power Supply	- Input voltage from step-up circuit. Connect to an external power supply of -4.5V to -6.6V.
VSSA	I	Ground	- System ground for the analog circuit In the case of COG, connect to GND on the FPC to prevent noise.
VSSREF	I	Ground	- System ground for the analog circuit In the case of COG, connect to GND on the FPC to prevent noise.
LVDSVSS	I	Ground	- System ground for MIPI DSI analog ground In the case of COG, connect to GND on the FPC to prevent noise.
VSS	I	Ground	- System ground for digital circuit In the case of COG, connect to GND on the FPC to prevent noise.
MTP_PWR	I	Power Supply	- Input power for OTP programming. MTP_PWR=8. 5V When not under programming, let MTP_PWR float or connect to ground.
DC-to-DC Circuit Pins			
VREG1OUT	O	Analog	- Regulator output voltage from VSP, It's for positive gray scale voltage. Connect to a stabilizing capacitor between GVDD and VSSA.
VREG2OUT	O	Analog	- Regulator output voltage from VSN, It's for negative gray scale voltage. Connect to a stabilizing capacitor between NGVDD and VSSA.
VCL	O	Analog	- Output voltage from step-up circuit

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			Connect to a stabilizing capacitor between VCL and VSSA.
VGH	O	Analog	- Output voltage from step-up circuit Connect to a stabilizing capacitor between VGH and VSSA.
VGL	O	Analog	- Output voltage from step-up circuit Connect to a stabilizing capacitor between VGL and VSSA.
VGLO1	O	Analog	- Negative power supply to panel GIP circuits If need different VGL voltage, must connect to a stabilizing capacitor between VGLO1 and VSSA.
EXTP	O	VCI	- Control signal output to generate VSP
EXTN	O	VCI	- Control signal output to generate VSN
LVDSVDD	O	Analog	- MIPI DSI regulator output
VREF	O	Analog	- Reference voltage from internal band gap circuit (1.8V typical)
VCORE	O	Analog	- Internal logic regulator output (1.5V typical) Connect to a stabilizing capacitor between VCORE and VSSA.
C21P/ C21N C22P / C22N	I/O	Step-up Capacitor	- Connect the charge-pumping capacitor for generating VGH level.
C23P / C23N C24P / C24N	I/O	Step-up Capacitor	- Connect the charge-pumping capacitor for generating VGL level.
C41P / C41N C42P / C42N	I/O	Step-up Capacitor	- Connect the charge-pumping capacitor for generating VCL level.
Test / Dummy Pins			
PCLK	I	VDDI	- Test pins Unused pins should be left open.
D[7:0]	I/O	VDDI	- Test pins Unused pins should be left open or connected to VSS, VDDI.
TEST[5:0]	I/O	VDDI	- Test pins Unused pins should be left open or connected to VSS, VDDI.
TOUT[3:0]	I/O	VDDI	- Test pins Unused pins should be left open or connected to VSS, VDDI.
VTESTOUTP	O	Analog	- Analog test output pin Let it open.
VTESTOUTN	O	Analog	- Analog test output pin Let it open.
CSX	I	VDDI	- Test pins Fix to VDDI or VSS level when not in use.
DCX	I	VDDI	- Test pins Fix to VDDI or VSS level when not in use.
SCL	I	VDDI	- Test pins Fix to VDDI or VSS level when not in use.
SDI	I	VDDI	- Test pins Leave the pin open when not in use.
SDO	O	VDDI	- Test pins Leave the pin open when not in use.
TE1	O	VDDI	- Test pins. Leave the pin open when not in use.
C31P	-	-	- Dummy pins Let it open.
VCOMR	-	-	- Dummy pins Let it open.
VGLO2DUMMY	-	-	- Dummy pins Let it open.
DUMMYR1	-	Analog	- dummy pins Propose to connect these two pads separately when use for bonding resistance measurement
VSSDUMMY	-	-	- Dummy pins Let it open.
DUMMY[85:3]	-	-	- Dummy pins Let it open.

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DUMMYN	-	-	- Dummy pins Let it open.
DUMMYP	-	-	- Dummy pins Let it open.

first FC components

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3.4. Pin Assignment

Chip Size: 27840 um x 875 um

Pad Location: Pad Center.

Coordinate Origin: Chip center

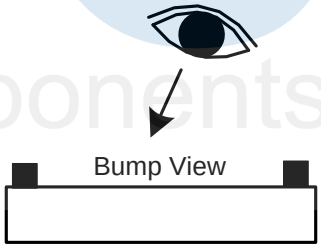
Bump Size:

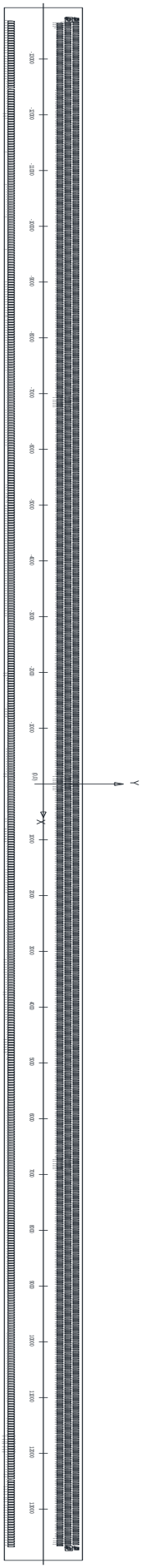
1. 30um x 73um

   Pad 1 to 608.

2. 16um x 65um

   Pad 609 to 3092.

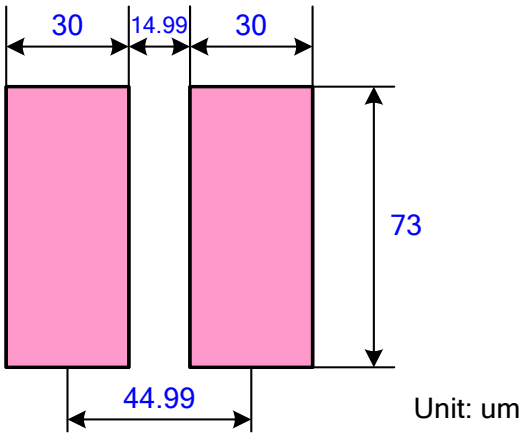
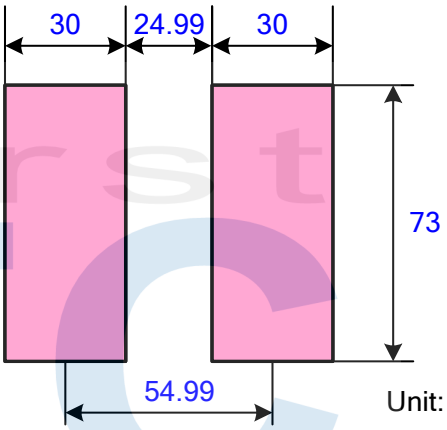
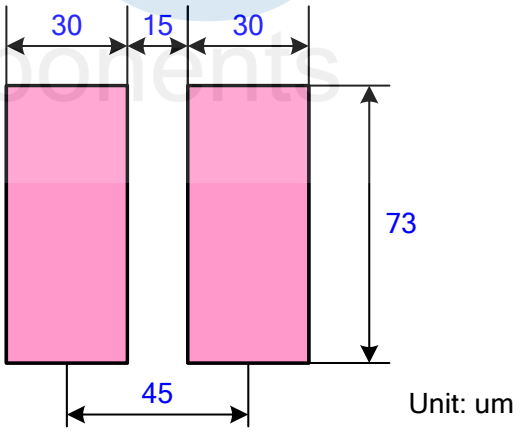




first FC components

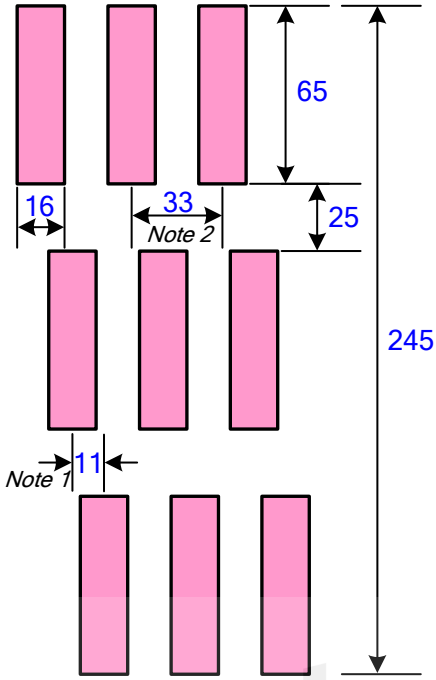
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3.5. Bump Arrangement

Input PAD (No. 1~27, 28~304, 305~581, 582~608)	
Input PAD (No. 27~28, 581~582)	
Input PAD (No. 304~305)	

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Output PAD
(No. 609~3092)

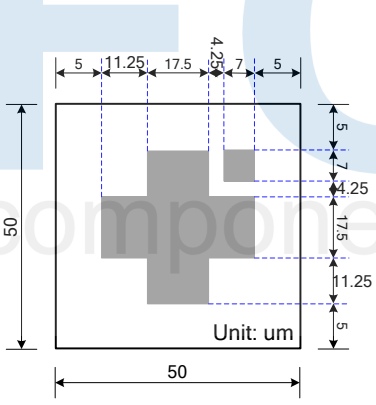


Notes:

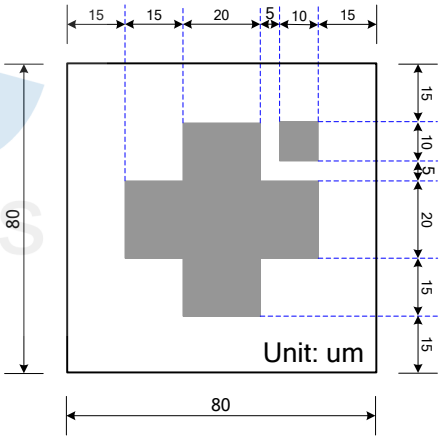
1. Pad has temperature compensation design, so the space may be 11um or 10.99um.

2. Pad has temperature compensation design, so the space may be 33um or 32.99um.

Alignment mark R

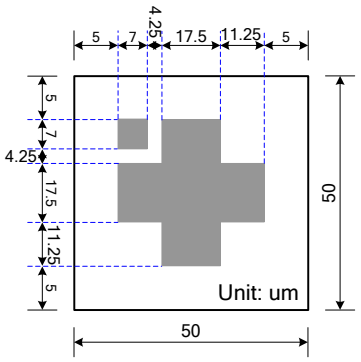
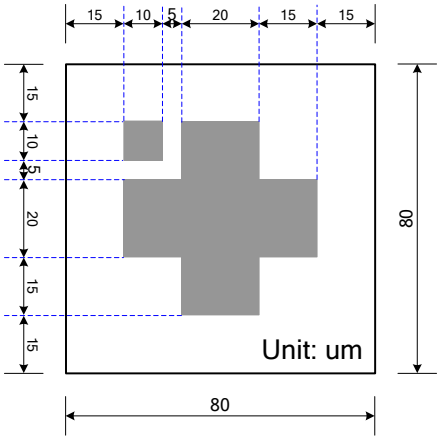


Alignment mark: (13706,372.5)



Alignment mark: (13706,285.5)

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Alignment mark L	 Alignment mark: (-13706,372.5)  Alignment mark: (-13706,285.5)

first FC components

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3.6. Pad Coordination

No.	Name	X	Y
1	DUMMY1	-13664.47	-361
2	DUMMY1	-13619.48	-361
3	GOUT_L1	-13574.49	-361
4	GOUT_L2	-13529.5	-361
5	GOUT_L3	-13484.51	-361
6	GOUT_L4	-13439.52	-361
7	GOUT_L5	-13394.53	-361
8	GOUT_L6	-13349.54	-361
9	GOUT_L7	-13304.55	-361
10	GOUT_L8	-13259.56	-361
11	GOUT_L9	-13214.57	-361
12	GOUT_L10	-13169.58	-361
13	GOUT_L11	-13124.59	-361
14	GOUT_L12	-13079.6	-361
15	GOUT_L13	-13034.61	-361
16	GOUT_L14	-12989.62	-361
17	GOUT_L15	-12944.63	-361
18	GOUT_L16	-12899.64	-361
19	GOUT_L17	-12854.65	-361
20	GOUT_L18	-12809.66	-361
21	GOUT_L19	-12764.67	-361
22	GOUT_L20	-12719.68	-361
23	GOUT_L21	-12674.69	-361
24	GOUT_L22	-12629.7	-361
25	VCOM	-12584.71	-361
26	VCOM	-12539.72	-361
27	VCOM	-12494.73	-361
28	VSSA	-12439.74	-361
29	VSSA	-12394.75	-361
30	VSSA	-12349.76	-361
31	VSSA	-12304.77	-361
32	VSSA	-12259.78	-361
33	VSSA	-12214.79	-361
34	VSSA	-12169.8	-361
35	VSSA	-12124.81	-361
36	VSSA	-12079.82	-361
37	VSSA	-12034.83	-361
38	VTESTOUTP	-11989.84	-361
39	VTESTOUTP	-11944.85	-361
40	LVDSVSS	-11899.86	-361
41	D0N	-11854.87	-361
42	D0N	-11809.88	-361
43	D0N	-11764.89	-361
44	D0N	-11719.9	-361
45	D0N	-11674.91	-361
46	D0N	-11629.92	-361
47	D0P	-11584.93	-361
48	D0P	-11539.94	-361
49	D0P	-11494.95	-361
50	D0P	-11449.96	-361
51	D0P	-11404.97	-361
52	D0P	-11359.98	-361
53	LVDSVSS	-11314.99	-361
54	D1N	-11270	-361
55	D1N	-11225.01	-361
56	D1N	-11180.02	-361
57	D1N	-11135.03	-361
58	D1N	-11090.04	-361
59	D1N	-11045.05	-361
60	D1P	-11000.06	-361
61	D1P	-10955.07	-361
62	D1P	-10910.08	-361
63	D1P	-10865.09	-361
64	D1P	-10820.1	-361
65	D1P	-10775.11	-361
66	LVDSVSS	-10730.12	-361
67	CLKN	-10685.13	-361
68	CLKN	-10640.14	-361
69	CLKN	-10595.15	-361
70	CLKN	-10550.16	-361
71	CLKN	-10505.17	-361
72	CLKN	-10460.18	-361
73	CLKP	-10415.19	-361
74	CLKP	-10370.2	-361
75	CLKP	-10325.21	-361
76	CLKP	-10280.22	-361
77	CLKP	-10235.23	-361
78	CLKP	-10190.24	-361
79	LVDSVSS	-10145.25	-361
80	D2N	-10100.26	-361
81	D2N	-10055.27	-361
82	D2N	-10010.28	-361
83	D2N	-9965.29	-361
84	D2N	-9920.3	-361
85	D2N	-9875.31	-361
86	D2P	-9830.32	-361
87	D2P	-9785.33	-361
88	D2P	-9740.34	-361
89	D2P	-9695.35	-361
90	D2P	-9650.36	-361
91	D2P	-9605.37	-361
92	LVDSVSS	-9560.38	-361
93	D3N	-9515.39	-361
94	D3N	-9470.4	-361
95	D3N	-9425.41	-361
96	D3N	-9380.42	-361
97	D3N	-9335.43	-361
98	D3N	-9290.44	-361
99	D3P	-9245.45	-361
100	D3P	-9200.46	-361
101	D3P	-9155.47	-361
102	D3P	-9110.48	-361
103	D3P	-9065.49	-361
104	D3P	-9020.5	-361
105	LVDSVSS	-8975.51	-361
106	LVDSVSS	-8930.52	-361
107	LVDSVSS	-8885.53	-361
108	LVDSVSS	-8840.54	-361
109	LVDSVSS	-8795.55	-361
110	LVDSVSS	-8750.56	-361
111	LVDSVSS	-8705.57	-361
112	LVDSVSS	-8660.58	-361
113	LVDSVSS	-8615.59	-361
114	LVDSVSS	-8570.6	-361
115	LVDSVSS	-8525.61	-361
116	LVDSVSS	-8480.62	-361
117	LVDSVDD	-8435.63	-361
118	LVDSVDD	-8390.64	-361
119	LVDSVDD	-8345.65	-361
120	LVDSVDD	-8300.66	-361
121	LVDSVDD	-8255.67	-361
122	LVDSVDD	-8210.68	-361
123	LVDSVDD	-8165.69	-361
124	LVDSVDD	-8120.7	-361
125	LVDSVDD	-8075.71	-361
126	LVDSVDD	-8030.72	-361
127	LVDSVDD	-7985.73	-361
128	LVDSVDD	-7940.74	-361
129	VDDAM	-7895.75	-361
130	VDDAM	-7850.76	-361
131	VDDAM	-7805.77	-361
132	VDDAM	-7760.78	-361
133	VDDAM	-7715.79	-361
134	VDDAM	-7670.8	-361
135	VDDAM	-7625.81	-361
136	VDDAM	-7580.82	-361
137	VDDAM	-7535.83	-361
138	VDDAM	-7490.84	-361
139	VDDAM	-7445.85	-361
140	VDDAM	-7400.86	-361
141	VCC1	-7355.87	-361
142	VCC1	-7310.88	-361
143	VCC1	-7265.89	-361
144	VCC1	-7220.9	-361
145	VCC1	-7175.91	-361
146	VCC1	-7130.92	-361
147	VCC1	-7085.93	-361
148	VCC1	-7040.94	-361
149	VCC1	-6995.95	-361
150	VCC1	-6950.96	-361
151	VCC1	-6905.97	-361
152	VCC1	-6860.98	-361
153	VCC1	-6815.99	-361
154	VCC1	-6771	-361
155	VCC1	-6726.01	-361
156	VCORE	-6681.02	-361
157	VCORE	-6636.03	-361
158	VCORE	-6591.04	-361
159	VCORE	-6546.05	-361
160	VCORE	-6501.06	-361
161	VCORE	-6456.07	-361
162	VCORE	-6411.08	-361
163	VCORE	-6366.09	-361
164	VCORE	-6321.1	-361
165	VCORE	-6276.11	-361
166	VCORE	-6231.12	-361
167	VCORE	-6186.13	-361
168	VCORE	-6141.14	-361
169	VCORE	-6096.15	-361
170	VCORE	-6051.16	-361
171	VSS	-6006.17	-361
172	VSS	-5961.18	-361
173	VSS	-5916.19	-361
174	VSS	-5871.2	-361
175	VSS	-5826.21	-361
176	VSS	-5781.22	-361
177	VSS	-5736.23	-361
178	VSS	-5691.24	-361
179	VSS	-5646.25	-361
180	VSS	-5601.26	-361
181	VSS	-5556.27	-361
182	VSS	-5511.28	-361
183	VSS	-5466.29	-361
184	VSS	-5421.3	-361
185	VSS	-5376.31	-361
186	TOUT3	-5331.32	-361
187	TOUT3	-5286.33	-361
188	TOUT2	-5241.34	-361
189	TOUT2	-5196.35	-361
190	TOUT1	-5151.36	-361
191	TOUT1	-5106.37	-361
192	TOUT0	-5061.38	-361
193	TOUT0	-5016.39	-361
194	DUMMYP	-4971.4	-361
195	DUMMYP	-4926.41	-361
196	DUMMYP	-4881.42	-361
197	DUMMYP	-4836.43	-361
198	DUMMYP	-4791.44	-361
199	DUMMYP	-4746.45	-361
200	DUMMYP	-4701.46	-361
201	DUMMYP	-4656.47	-361
202	DUMMYP	-4611.48	-361
203	DUMMYP	-4566.49	-361
204	DUMMYP	-4521.5	-361
205	DUMMYP	-4476.51	-361
206	DUMMYP	-4431.52	-361
207	DUMMYP	-4386.53	-361
208	DUMMYP	-4341.54	-361
209	DUMMYP	-4296.55	-361
210	DUMMYP	-4251.56	-361
211	DUMMYP	-4206.57	-361
212	DUMMYP	-4161.58	-361
213	DUMMYP	-4116.59	-361
214	DUMMYP	-4071.6	-361
215	DUMMYP	-4026.61	-361
216	DUMMYP	-3981.62	-361
217	DUMMYP	-3936.63	-361
218	DUMMYP	-3891.64	-361
219	DUMMYP	-3846.65	-361
220	DUMMYP	-3801.66	-361
221	DUMMYP	-3756.67	-361
222	DUMMYP	-3711.68	-361
223	DUMMYP	-3666.69	-361
224	DUMMYP	-3621.7	-361
225	DUMMYP	-3576.71	-361
226	DUMMYP	-3531.72	-361
227	DUMMYP	-3486.73	-361
228	DUMMYP	-3441.74	-361
229	DUMMYP	-3396.75	-361
230	DUMMYP	-3351.76	-361
231	DUMMYP	-3306.77	-361
232	DUMMYP	-3261.78	-361
233	DUMMYP	-3216.79	-361
234	DUMMYP	-3171.8	-361
235	DUMMYP	-3126.81	-361
236	DUMMYP	-3081.82	-361
237	DUMMYP	-3036.83	-361
238	DUMMYP	-2991.84	-361
239	VSS	-2946.85	-361
240	VSS	-2901.86	-361
241	D7	-2856.87	-361
242	D7	-2811.88	-361
243	D6	-2766.89	-361
244	D6	-2721.9	-361
245	D5	-2676.91	-361
246	D5	-2631.92	-361
247	D4	-2586.93	-361
248	D4	-2541.94	-361
249	D3	-2496.95	-361
250	D3	-2451.96	-361
251	D2	-2406.97	-361
252	D2	-2361.98	-361
253	D1	-2316.99	-361
254	D1	-2272	-361
255	D0	-2227.01	-361
256	D0	-2182.02	-361
257	HS	-2137.03	-361
258	HS	-2092.04	-361
259	VS	-2047.05	-361
260	VS	-2002.06	-361
261	VSSDUMMY	-1957.07	-361
262	VSSDUMMY	-1912.08	-361
263	PCLK	-1867.09	-361
264	PCLK	-1822.1	-361
265	DCX	-1777.11	-361
266	DCX	-1732.12	-361
267	CSX	-1687.13	-361
268	CSX	-1642.14	-361
269	SCL	-1597.15	-361
270	SCL	-1552.16	-361
271	SDI	-1507.17	-361
272	SDI	-1462.18	-361
273	SDO	-1417.19	-361
274	SDO	-1372.2	-361
275	LEDPWM	-1327.21	-361
276	LEDPWM	-1282.22	-361
277	LEDPWM	-1237.23	-361
278	LEDPWM	-1192.24	-361
279	TE	-1147.25	-361
280	TE	-1102.26	-361
281	TE	-1057.27	-361
282	TE	-1012.28	-361
283	TE	-967.29	-361
284	TE	-922.3	-361
285	TE1	-877.31	-361
286	TE1	-832.32	-361
287	TE1	-787.33	-361
288	TE1	-742.34	-361
289	TE1	-697.35	-361
290	TE1	-652.36	-361
291	RESX	-607.37	-361
292	RESX	-562.38	-361
293	RESX	-517.39	-361
294	RESX	-472.4	-361
295	TEST5	-427.41	-361
296	TEST4	-382.42	-361
297	TEST3	-337.43	-361
298	TEST2	-292.44	-361
299	TEST1	-247.45	-361
300	TEST0	-202.46	-361
301	VSSDUMMY	-157.47	-361
302	VSSDUMMY	-112.48	-361
303	IM0	-67.49	-361
304	IM0	-22.5	-361
305	VDDI	22.5	-361
306	VDDI	67.49	-361
307	IM1	112.48	-361
308	IM1	157.47	-361
309	IM2	202.46	-361
310	IM2	247.45	-361
311	RS0	292.44	-361
312	RS0	337.43	-361
313	VDDI	382.42	-361
314	VDDI	427.41	-361
315	RS1	472.4	-361
316	RS1	517.39	-361
317	VSS	562.38	-361
318	VSS	607.37	-361
319	LANSEL	652.36	-361
320	LANSEL	697.35	-361
321	VDDI	742.34	-361
322	VDDI	787.33	-361
323	BOOSTM0	832.32	-361
324	BOOSTM0	877.31	-361
325	BOOSTM2	922.3	-361
326	BOOSTM2	967.29	-361
327	BOOSTM1	1012.28	-361
328	BOOSTM1	1057.27	-361
329	VCC2	1102.26	-361
330	VCC2	1147.25	-361
331	VCC2	1192.24	-361
332	VCC2	1237.23	-361
333	VCC2	1282.22	-361
334	VCC2	1327.21	-361
335	VCC2	1372.2	-361
336	VCC2	1417.19	-361
337	VCC2	1462.18	-361
338	VCC2	1507.17	-361
339	VCORE	1552.16	-361
340	VCORE	1597.15	-361
341	VCORE	1642.14	-361
342	VCORE	1687.13	-361
343	VCORE	1732.12	-361
344	VCORE	1777.11	-361
345	VCORE	1822.1	-361
346	VCORE	1867.09	-361
347	VCORE	1912.08	-361
348	VCORE	1957.07	-361
349	VSS	2002.06	-361
350	VSS	2047.05	-361
351	VSS	2092.04	-361
352	VSS	2137.03	-361
353	VSS	2182.02	-361
354	VSS	2227.01	-361
355	VSS	2272	-361
356	VSS	2316.99	-361
357	VSS	2361.98	-361
358	VSS	2406.97	-361
359	EXTN	2451.96	-361
360	EXTN	2496.95	-361
361	EXTN	2541.94	-361
362	EXTN	2586.93	-361
363	EXTN	2631.92	-361
364	EXTN	2676.91	-361
365	EXTN	2721.9	-361
366	EXTN	2766.89	-361
367	EXTP	2811.88	-361
368	EXTP	2856.87	-361
369	EXTP	2901.86	-361
370	EXTP	2946.85	-361
371	EXTP	2991.84	-361
372	EXTP	3036.83	-361
373	EXTP	3081.82	-361
374	EXTP	3126.81	-361
375	MTP_PWR	3171.8	-361
376	MTP_PWR	3216.79	-361
377	MTP_PWR	3261.78	-361
378	MTP_PWR	3306.77	-361
379	MTP_PWR	3351.76	-361
380	MTP_PWR	3396.75	-361
381	DUMMYN	3441.74	-361
382	DUMMYN	3486.73	-361
383	VCIREF	3531.72	-361
384	VCIREF	3576.71	-361
385	VCIREF	3621.7	-361
386	VCIREF	3666.69	-361
387	VCIREF	3711.68	-361
388	VTESTOUTN	3756.67	-361
389	VTESTOUTN	3801.66	-361
390	DUMMYN	3846.65	-361
391	DUMMYN	3891.64	-361
392	DUMMYN	3936.63	-361
393	DUMMYN	3981.62	-361
394	DUMMYN	4026.61	-361
395	DUMMYN	4071.6	-361
396	VSSREF	4116.59	-361
397	VSSREF	4161.58	-361
398	VSSREF	4206.57	-361
399	VSSREF	4251.56	-361
400	VSSA	4296.55	-361

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408	VREG1OUT	4656.47	-361
409	VREG1OUT	4701.46	-361
410	VREG2OUT	4746.45	-361
411	VREG2OUT	4791.44	-361
412	VREG2OUT	4836.43	-361
413	VREF	4881.42	-361
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415	VREF	4971.4	-361
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943	S2078	9980.23	275
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946	S2075	9947.24	275
947	S2074	9936.24	365
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1111	S1910	8132.65	275
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1510	S1529	3744.65	275
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1600	S1439	2754.87	275

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1811	S1228	434.4	365
1812	S1227	423.4	185
1813	S1226	412.4	275
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1815	S1224	390.41	185
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1819	S1220	346.42	275
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1822	S1217	313.43	275
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1825	S1214	280.43	275
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1832	S1207	203.45	365
1833	S1206	192.45	185
1834	S1205	181.46	275
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1836	S1203	159.46	185
1837	S1202	148.46	275
1838	S1201	137.47	365
1839	DUMMY29	126.47	185
1840	DUMMY30	115.47	275
1841	DUMMY31	104.47	365
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1843	DUMMY33	82.48	275
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1846	DUMMY36	49.49	275
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1852	DUMMY42	-16.49	275
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1862	DUMMY52	-126.47	365
1863	S1200	-137.47	185
1864	S1199	-148.46	275
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1867	S1196	-181.46	275
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1871	S1192	-225.45	365
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1911	S1152	-665.35	185
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1913	S1150	-687.34	365
1914	S1149	-698.34	185
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1916	S1147	-720.33	365
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1918	S1145	-742.33	275
1919	S1144	-753.33	365
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1925	S1138	-819.31	365
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1927	S1136	-841.31	275
1928	S1135	-852.3	365
1929	S1134	-863.3	185
1930	S1133	-874.3	275
1931	S1132	-885.3	365
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1933	S1130	-907.29	275
1934	S1129	-918.29	365
1935	S1128	-929.29	185
1936	S1127	-940.28	275
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1938	S1125	-962.28	185
1939	S1124	-973.28	275
1940	S1123	-984.27	365
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1942	S1121	-1006.27	275
1943	S1120	-1017.27	365
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1945	S1118	-1039.26	275
1946	S1117	-1050.26	365
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1948	S1115	-1072.25	275
1949	S1114	-1083.25	365
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1951	S1112	-1105.25	275
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1958	S1105	-1182.23	365
1959	S1104	-1193.23	185
1960	S1103	-1204.22	275
1961	S1102	-1215.22	365
1962	S1101	-1226.22	185
1963	S1100	-1237.22	275
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1966	S1097	-1270.21	275
1967	S1096	-1281.21	365
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1972	S1091	-1336.19	275
1973	S1090	-1347.19	365
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1981	S1082	-1435.17	275
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1983	S1080	-1457.17	185
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1988	S1075	-1512.15	365
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1994	S1069	-1578.14	365
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1999	S1064	-1633.13	275
2000	S1063	-1644.12	365

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2007	S1056	-1721.11	185
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2009	S1054	-1743.1	365
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2011	S1052	-1765.1	275
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2017	S1046	-1831.08	275
2018	S1045	-1842.08	365
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2020	S1043	-1864.07	275
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2040	S1023	-2084.02	185
2041	S1022	-2095.02	275
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2066	S997	-2369.96	365
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2075	S988	-2468.94	365
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2078	S985	-2501.93	365
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2109	S954	-2842.85	185
2110	S953	-2853.85	275
2111	S952	-2864.85	365
2112	S951	-2875.84	185
2113	S950	-2886.84	275
2114	S949	-2897.84	365
2115	S948	-2908.84	185
2116	S947	-2919.83	275
2117	S946	-2930.83	365
2118	S945	-2941.83	185
2119	S944	-2952.83	275
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2121	S942	-2974.82	185
2122	S941	-2985.82	275
2123	S940	-2996.82	365
2124	S939	-3007.81	185
2125	S938	-3018.81	275
2126	S937	-3029.81	365
2127	S936	-3040.81	185
2128	S935	-3051.8	275
2129	S934	-3062.8	365
2130	S933	-3073.8	185
2131	S932	-3084.8	275
2132	S931	-3095.79	365
2133	S930	-3106.79	185
2134	S929	-3117.79	275
2135	S928	-3128.79	365
2136	S927	-3139.78	185
2137	S926	-3150.78	275
2138	S925	-3161.78	365
2139	S924	-3172.78	185
2140	S923	-3183.77	275
2141	S922	-3194.77	365
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2163	S900	-3436.72	185
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2172	S891	-3535.69	185
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2179	S884	-3612.68	275
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2182	S881	-3645.67	275
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2192	S871	-3755.64	365
2193	S870	-3766.64	185
2194	S869	-3777.64	275
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2196	S867	-3799.63	185
2197	S866	-3810.63	275
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2206	S857	-3909.61	275
2207	S856	-3920.61	365
2208	S855	-3931.6	185
2209	S854	-3942.6	275
2210	S853	-3953.6	365
2211	S852	-3964.6	185
2212	S851	-3975.59	275
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2215	S848	-4008.59	275
2216	S847	-4019.58	365
2217	S846	-4030.58	185
2218	S845	-4041.58	275
2219	S844	-4052.58	365
2220	S843	-4063.57	185
2221	S842	-4074.57	275
2222	S841	-4085.57	365
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2225	S838	-4118.56	365
2226	S837	-4129.56	185
2227	S836	-4140.56	275
2228	S835	-4151.55	365
2229	S834	-4162.55	185
2230	S833	-4173.55	275
2231	S832	-4184.55	365
2232	S831	-4195.54	185
2233	S830	-4206.54	275
2234	S829	-4217.54	365
2235	S828	-4228.54	185
2236	S827	-4239.53	275
2237	S826	-4250.53	365
2238	S825	-4261.53	185
2239	S824	-4272.53	275
2240	S823	-4283.52	365
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2243	S820	-4316.52	365
2244	S819	-4327.51	185
2245	S818	-4338.51	275
2246	S817	-4349.51	365
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2280	S783	-4723.42	185
2281	S782	-4734.42	275
2282	S781	-4745.42	365
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2285	S778	-4778.41	365
2286	S777	-4789.41	185
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2290	S773	-4833.4	275
2291	S772	-4844.4	365
2292	S771	-4855.39	185
2293	S770	-4866.39	275
2294	S769	-4877.39	365
2295	S768	-4888.39	185
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2297	S766	-4910.38	365
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2307	S756	-5020.36	185
2308	S755	-5031.35	275
2309	S754	-5042.35	365
2310	S753	-5053.35	185
2311	S752	-5064.35	275
2312	S751	-5075.34	365
2313	S750	-5086.34	185
2314	S749	-5097.34	275
2315	S748	-5108.34	365
2316	S747	-5119.33	185
2317	S746	-5130.33	275
2318	S745	-5141.33	365
2319	S744	-5152.33	185
2320	S743	-5163.32	275
2321	S742	-5174.32	365
2322	S741	-5185.32	185
2323	S740	-5196.32	275
2324	S739	-5207.31	365
2325	S738	-5218.31	185
2326	S737	-5229.31	275
2327	S736	-5240.31	365
2328	S735	-5251.3	185
2329	S734	-5262.3	275
2330	S733	-5273.3	365
2331	S732	-5284.3	185
2332	S731	-5295.29	275
2333	S730	-5306.29	365
2334	S729	-5317.29	185
2335	S728	-5328.29	275
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2339	S724	-5372.28	365
2340	S723	-5383.27	185
2341	S722	-5394.27	275
2342	S721	-5405.27	365
2343	S720	-5416.27	185
2344	S719	-5427.26	275
2345	S718	-5438.26	365
2346	S717	-5449.26	185
2347	S716	-5460.26	275
2348	S715	-5471.25	365
2349	S714	-5482.25	185
2350	S713	-5493.25	275
2351	S712	-5504.25	365
2352	S711	-5515.24	185
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2354	S709	-5537.24	365
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2356	S707	-5559.23	275
2357	S706	-5570.23	365
2358	S705	-5581.23	185
2359	S704	-5592.23	275
2360	S703	-5603.22	365
2361	S702	-5614.22	185
2362	S701	-5625.22	275
2363	S700	-5636.22	365
2364	S699	-5647.21	185
2365	S698	-5658.21	275
2366	S697	-5669.21	365
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2375	S688	-5768.19	365
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2378	S685	-5801.18	365
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2381	S682	-5834.17	365
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2383	S680	-5856.17	275
2384	S679	-5867.16	365
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2387	S676	-5900.16	365
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2389	S674	-5922.15	275
2390	S673	-5933.15	365
2391	S672	-5944.15	185
2392	S671	-5955.14	275
2393	S670	-5966.14	365
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2396	S667	-5999.13	365
2397	S666	-6010.13	185
2398	S665	-6021.13	275
2399	S664	-6032.13	365
2400	S663	-6043.12	185

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2414	S649	-6197.09	365
2415	S648	-6208.09	185
2416	S647	-6219.08	275
2417	S646	-6230.08	365
2418	S645	-6241.08	185
2419	S644	-6252.08	275
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2422	S641	-6285.07	275
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2429	S634	-6362.05	365
2430	S633	-6373.05	185
2431	S632	-6384.05	275
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2433	S630	-6406.04	185
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2435	S628	-6428.04	365
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2437	S626	-6450.03	275
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2442	S621	-6505.02	185
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2445	S618	-6538.01	185
2446	S617	-6549.01	275
2447	S616	-6560.01	365
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2462	S601	-6724.97	365
2463	DUMMY53	-6735.97	185
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2469	DUMMY59	-6801.95	185
2470	DUMMY60	-6812.95	275
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2480	DUMMY70	-6922.92	365
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2492	S589	-7054.89	365
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2507	S574	-7219.86	365
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2509	S572	-7241.85	275
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2512	S569	-7274.84	275
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2514	S567	-7296.84	185
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2517	S564	-7329.83	185
2518	S563	-7340.83	275
2519	S562	-7351.83	365
2520	S561	-7362.82	185
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2523	S558	-7395.82	185
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2525	S556	-7417.81	365
2526	S555	-7428.81	185
2527	S554	-7439.81	275
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2529	S552	-7461.8	185
2530	S551	-7472.8	275
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2535	S546	-7527.79	185
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2537	S544	-7549.78	365
2538	S543	-7560.78	185
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2563	S518	-7835.72	275
2564	S517	-7846.71	365
2565	S516	-7857.71	185
2566	S515	-7868.71	275
2567	S514	-7879.71	365
2568	S513	-7890.7	185
2569	S512	-7901.7	275
2570	S511	-7912.7	365
2571	S510	-7923.7	185
2572	S509	-7934.69	275
2573	S508	-7945.69	365
2574	S507	-7956.69	185
2575	S506	-7967.69	275
2576	S505	-7978.68	365
2577	S504	-7989.68	185
2578	S503	-8000.68	275
2579	S502	-8011.68	365
2580	S501	-8022.67	185
2581	S500	-8033.67	275
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2583	S498	-8055.67	185
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2586	S495	-8088.66	185
2587	S494	-8099.66	275
2588	S493	-8110.65	365
2589	S492	-8121.65	185
2590	S491	-8132.65	275
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2592	S489	-8154.64	185
2593	S488	-8165.64	275
2594	S487	-8176.64	365
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2597	S484	-8209.63	365
2598	S483	-8220.63	185
2599	S482	-8231.63	275
2600	S481	-8242.62	365

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2604	S477	-8286.61	185
2605	S476	-8297.61	275
2606	S475	-8308.61	365
2607	S474	-8319.61	185
2608	S473	-8330.6	275
2609	S472	-8341.6	365
2610	S471	-8352.6	185
2611	S470	-8363.6	275
2612	S469	-8374.59	365
2613	S468	-8385.59	185
2614	S467	-8396.59	275
2615	S466	-8407.59	365
2616	S465	-8418.58	185
2617	S464	-8429.58	275
2618	S463	-8440.58	365
2619	S462	-8451.58	185
2620	S461	-8462.57	275
2621	S460	-8473.57	365
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2623	S458	-8495.57	275
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2625	S456	-8517.56	185
2626	S455	-8528.56	275
2627	S454	-8539.56	365
2628	S453	-8550.55	185
2629	S452	-8561.55	275
2630	S451	-8572.55	365
2631	S450	-8583.55	185
2632	S449	-8594.54	275
2633	S448	-8605.54	365
2634	S447	-8616.54	185
2635	S446	-8627.54	275
2636	S445	-8638.53	365
2637	S444	-8649.53	185
2638	S443	-8660.53	275
2639	S442	-8671.53	365
2640	S441	-8682.52	185
2641	S440	-8693.52	275
2642	S439	-8704.52	365
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2646	S435	-8748.51	185
2647	S434	-8759.51	275
2648	S433	-8770.5	365
2649	S432	-8781.5	185
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2651	S430	-8803.5	365
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2657	S424	-8869.48	365
2658	S423	-8880.48	185
2659	S422	-8891.48	275
2660	S421	-8902.47	365
2661	S420	-8913.47	185
2662	S419	-8924.47	275
2663	S418	-8935.47	365
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2679	S402	-9111.43	185
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2683	S398	-9155.42	275
2684	S397	-9166.41	365
2685	S396	-9177.41	185
2686	S395	-9188.41	275
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2690	S391	-9232.4	365
2691	S390	-9243.4	185
2692	S389	-9254.39	275
2693	S388	-9265.39	365
2694	S387	-9276.39	185
2695	S386	-9287.39	275
2696	S385	-9298.38	365
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2706	S375	-9408.36	185
2707	S374	-9419.36	275
2708	S373	-9430.35	365
2709	S372	-9441.35	185
2710	S371	-9452.35	275
2711	S370	-9463.35	365
2712	S369	-9474.34	185
2713	S368	-9485.34	275
2714	S367	-9496.34	365
2715	S366	-9507.34	185
2716	S365	-9518.33	275
2717	S364	-9529.33	365
2718	S363	-9540.33	185
2719	S362	-9551.33	275
2720	S361	-9562.32	365
2721	S360	-9573.32	185
2722	S359	-9584.32	275
2723	S358	-9595.32	365
2724	S357	-9606.31	185
2725	S356	-9617.31	275
2726	S355	-9628.31	365
2727	S354	-9639.31	185
2728	S353	-9650.3	275
2729	S352	-9661.3	365
2730	S351	-9672.3	185
2731	S350	-9683.3	275
2732	S349	-9694.29	365
2733	S348	-9705.29	185
2734	S347	-9716.29	275
2735	S346	-9727.29	365
2736	S345	-9738.28	185
2737	S344	-9749.28	275
2738	S343	-9760.28	365
2739	S342	-9771.28	185
2740	S341	-9782.27	275
2741	S340	-9793.27	365
2742	S339	-9804.27	185
2743	S338	-9815.27	275
2744	S337	-9826.26	365
2745	S336	-9837.26	185
2746	S335	-9848.26	275
2747	S334	-9859.26	365
2748	S333	-9870.25	185
2749	S332	-9881.25	275
2750	S331	-9892.25	365
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2754	S327	-9936.24	185
2755	S326	-9947.24	275
2756	S325	-9958.23	365
2757	S324	-9969.23	185
2758	S323	-9980.23	275
2759	S322	-9991.23	365
2760	S321	-10002.22	185
2761	S320	-10013.22	275
2762	S319	-10024.22	365
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2764	S317	-10046.21	275
2765	S316	-10057.21	365
2766	S315	-10068.21	185
2767	S314	-10079.21	275
2768	S313	-10090.2	365
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2771	S310	-10123.2	365
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2773	S308	-10145.19	275
2774	S307	-10156.19	365
2775	S306	-10167.19	185
2776	S305	-10178.18	275
2777	S304	-10189.18	365
2778	S303	-10200.18	185
2779	S302	-10211.18	275
2780	S301	-10222.17	365
2781	S300	-10233.17	185
2782	S299	-10244.17	275
2783	S298	-10255.17	365
2784	S297	-10266.16	185
2785	S296	-10277.16	275
2786	S295	-10288.16	365
2787	S294	-10299.16	185
2788	S293	-10310.15	275
2789	S292	-10321.15	365
2790	S291	-10332.15	185
2791	S290	-10343.15	275
2792	S289	-10354.14	365
2793	S288	-10365.14	185
2794	S287	-10376.14	275
2795	S286	-10387.14	365
2796	S285	-10398.13	185
2797	S284	-10409.13	275
2798	S283	-10420.13	365
2799	S282	-10431.13	185
2800	S281	-10442.12	275

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2804	S277	-10486.11	365
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2807	S274	-10519.11	365
2808	S273	-10530.1	185
2809	S272	-10541.1	275
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2811	S270	-10563.1	185
2812	S269	-10574.09	275
2813	S268	-10585.09	365
2814	S267	-10596.09	185
2815	S266	-10607.09	275
2816	S265	-10618.08	365
2817	S264	-10629.08	185
2818	S263	-10640.08	275
2819	S262	-10651.08	365
2820	S261	-10662.07	185
2821	S260	-10673.07	275
2822	S259	-10684.07	365
2823	S258	-10695.07	185
2824	S257	-10706.06	275
2825	S256	-10717.06	365
2826	S255	-10728.06	185
2827	S254	-10739.06	275
2828	S253	-10750.05	365
2829	S252	-10761.05	185
2830	S251	-10772.05	275
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2832	S249	-10794.04	185
2833	S248	-10805.04	275
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2837	S244	-10849.03	365
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2849	S232	-10981	365
2850	S231	-10992	185
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2856	S225	-11057.98	185
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2861	S220	-11112.97	365
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2863	S218	-11134.97	275
2864	S217	-11145.96	365
2865	S216	-11156.96	185
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2869	S212	-11200.95	275
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2875	S206	-11266.94	275
2876	S205	-11277.93	365
2877	S204	-11288.93	185
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2879	S202	-11310.93	365
2880	S201	-11321.92	185
2881	S200	-11332.92	275
2882	S199	-11343.92	365
2883	S198	-11354.92	185
2884	S197	-11365.91	275
2885	S196	-11376.91	365
2886	S195	-11387.91	185
2887	S194	-11398.91	275
2888	S193	-11409.9	365
2889	S192	-11420.9	185
2890	S191	-11431.9	275
2891	S190	-11442.9	365
2892	S189	-11453.89	185
2893	S188	-11464.89	275
2894	S187	-11475.89	365
2895	S186	-11486.89	185
2896	S185	-11497.88	275
2897	S184	-11508.88	365
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2907	S174	-11618.86	185
2908	S173	-11629.85	275
2909	S172	-11640.85	365
2910	S171	-11651.85	185
2911	S170	-11662.85	275
2912	S169	-11673.84	365
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2917	S164	-11728.83	275
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2919	S162	-11750.83	185
2920	S161	-11761.82	275
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2922	S159	-11783.82	185
2923	S158	-11794.82	275
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2925	S156	-11816.81	185
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2927	S154	-11838.81	365
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2930	S151	-11871.8	365
2931	S150	-11882.8	185
2932	S149	-11893.79	275
2933	S148	-11904.79	365
2934	S147	-11915.79	185
2935	S146	-11926.79	275
2936	S145	-11937.78	365
2937	S144	-11948.78	185
2938	S143	-11959.78	275
2939	S142	-11970.78	365
2940	S141	-11981.77	185
2941	S140	-11992.77	275
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2943	S138	-12014.77	185
2944	S137	-12025.76	275
2945	S136	-12036.76	365
2946	S135	-12047.76	185
2947	S134	-12058.76	275
2948	S133	-12069.75	365
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2950	S131	-12091.75	275
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2952	S129	-12113.74	185
2953	S128	-12124.74	275
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2958	S123	-12179.73	185
2959	S122	-12190.73	275
2960	S121	-12201.72	365
2961	S120	-12212.72	185
2962	S119	-12223.72	275
2963	S118	-12234.72	365
2964	S117	-12245.71	185
2965	S116	-12256.71	275
2966	S115	-12267.71	365
2967	S114	-12278.71	185
2968	S113	-12289.7	275
2969	S112	-12300.7	365
2970	S111	-12311.7	185
2971	S110	-12322.7	275
2972	S109	-12333.69	365
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2976	S105	-12377.68	185
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2981	S100	-12432.67	365
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2989	S92	-12520.65	275
2990	S91	-12531.65	365
2991	S90	-12542.65	185
2992	S89	-12553.64	275
2993	S88	-12564.64	365
2994	S87	-12575.64	185
2995	S86	-12586.64	275
2996	S85	-12597.63	365
2997	S84	-12608.63	185
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2999	S82	-12630.63	365
3000	S81	-12641.62	185

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3004	S77	-12685.61	275
3005	S76	-12696.61	365
3006	S75	-12707.61	185
3007	S74	-12718.61	275
3008	S73	-12729.6	365
3009	S72	-12740.6	185
3010	S71	-12751.6	275
3011	S70	-12762.6	365
3012	S69	-12773.59	185
3013	S68	-12784.59	275
3014	S67	-12795.59	365
3015	S66	-12806.59	185
3016	S65	-12817.58	275
3017	S64	-12828.58	365
3018	S63	-12839.58	185
3019	S62	-12850.58	275
3020	S61	-12861.57	365
3021	S60	-12872.57	185
3022	S59	-12883.57	275
3023	S58	-12894.57	365
3024	S57	-12905.56	185
3025	S56	-12916.56	275
3026	S55	-12927.56	365
3027	S54	-12938.56	185
3028	S53	-12949.55	275
3029	S52	-12960.55	365
3030	S51	-12971.55	185
3031	S50	-12982.55	275
3032	S49	-12993.54	365
3033	S48	-13004.54	185
3034	S47	-13015.54	275
3035	S46	-13026.54	365
3036	S45	-13037.53	185
3037	S44	-13048.53	275
3038	S43	-13059.53	365
3039	S42	-13070.53	185
3040	S41	-13081.52	275
3041	S40	-13092.52	365
3042	S39	-13103.52	185
3043	S38	-13114.52	275
3044	S37	-13125.51	365
3045	S36	-13136.51	185
3046	S35	-13147.51	275
3047	S34	-13158.51	365
3048	S33	-13169.5	185
3049	S32	-13180.5	275
3050	S31	-13191.5	365
3051	S30	-13202.5	185
3052	S29	-13213.49	275
3053	S28	-13224.49	365
3054	S27	-13235.49	185
3055	S26	-13246.49	275
3056	S25	-13257.48	365
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3058	S23	-13279.48	275
3059	S22	-13290.48	365
3060	S21	-13301.47	185
3061	S20	-13312.47	275
3062	S19	-13323.47	365
3063	S18	-13334.47	185
3064	S17	-13345.46	275
3065	S16	-13356.46	365
3066	S15	-13367.46	185
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3068	S13	-13389.45	365
3069	S12	-13400.45	185
3070	S11	-13411.45	275
3071	S10	-13422.45	365
3072	S9	-13433.44	185
3073	S8	-13444.44	275
3074	S7	-13455.44	365
3075	S6	-13466.44	185
3076	S5	-13477.43	275
3077	S4	-13488.43	365
3078	S3	-13499.43	185
3079	S2	-13510.43	275
3080	S1	-13521.42	365
3081	SDUM1	-13532.42	185
3082	SDUM0	-13543.42	275
3083	DUMMY73	-13554.42	365
3084	DUMMY74	-13565.41	185
3085	DUMMY75	-13576.41	275
3086	DUMMY76	-13587.41	365
3087	DUMMY77	-13598.41	185
3088	DUMMY78	-13609.4	275
3089	DUMMY79	-13620.4	365
3090	DUMMY83	-13631.4	185
3091	DUMMY84	-13642.4	275
3092	DUMMY85	-13653.39	365
3093	Alignment mark L1	13706	372.5
3094	Alignment mark L2	13706	285.5
3095	Alignment mark R1	-13706	372.5
3096	Alignment mark R2	-13706	285.5

No.	Name	X	Y

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4. System Interface

4.1. DSI System Interface

4.1.1. General Description

The pad mapping of MIPI DSI interface is set by IM[2:0] pin, LANSEL pins and MIPI_LANE_SEL register(as below table).

Table 2: DSI Interface Lane Mode Selection

External Pad Set				Register	Configuration of MIPI Lane				
LANSEL	IM2	IM1	IM0	Page4_R00h MIPI_LANE_SEL	D0P/N Pin	D1P/N Pin	CLKP/N Pin	D2P/N Pin	D3P/N Pin
0	0	0	0	1	D3P/N	D2P/N	CLKP/N	D1P/N	D0P/N
0	0	0	1	1	D3N/P	D2N/P	CLKN/P	D1N/P	D0N/P
0	0	1	0	1	D0P/N	D1P/N	CLKP/N	D2P/N	D3P/N
0	0	1	1	1	D0N/P	D1N/P	CLKN/P	D2N/P	D3N/P
0	1	0	0	1	D3P/N	D0P/N	CLKP/N	D1P/N	D2P/N
0	1	0	1	1	D3N/P	D0N/P	CLKN/P	D1N/P	D2N/P
0	1	1	0	1	D2P/N	D1P/N	CLKP/N	D0P/N	D3P/N
0	1	1	1	1	D2N/P	D1N/P	CLKN/P	D0N/P	D3N/P
1	0	0	0	1	-	-	CLKP/N	D1P/N	D0P/N
1	0	0	1	1	-	-	CLKN/P	D1N/P	D0N/P
1	0	1	0	1	D0P/N	D1P/N	CLKP/N	-	-
1	0	1	1	1	D0N/P	D1N/P	CLKN/P	-	-
1	1	0	0	1	-	D0P/N	CLKP/N	D1P/N	-
1	1	0	1	1	-	D0N/P	CLKN/P	D1N/P	-
1	1	1	0	1	-	D1P/N	CLKP/N	D0P/N	-
1	1	1	1	1	-	D1N/P	CLKN/P	D0N/P	-
0	0	0	0	0	-	D2P/N	CLKP/N	D1P/N	D0P/N
0	0	0	1	0	-	D2N/P	CLKN/P	D1N/P	D0N/P
0	0	1	0	0	D0P/N	D1P/N	CLKP/N	D2P/N	-
0	0	1	1	0	D0N/P	D1N/P	CLKN/P	D2N/P	-
0	1	0	0	0	-	D0P/N	CLKP/N	D1P/N	D2P/N
0	1	0	1	0	-	D0N/P	CLKN/P	D1N/P	D2N/P
0	1	1	0	0	D2P/N	D1P/N	CLKP/N	D0P/N	-
0	1	1	1	0	D2N/P	D1N/P	CLKN/P	D0N/P	-
Others					Reserved				

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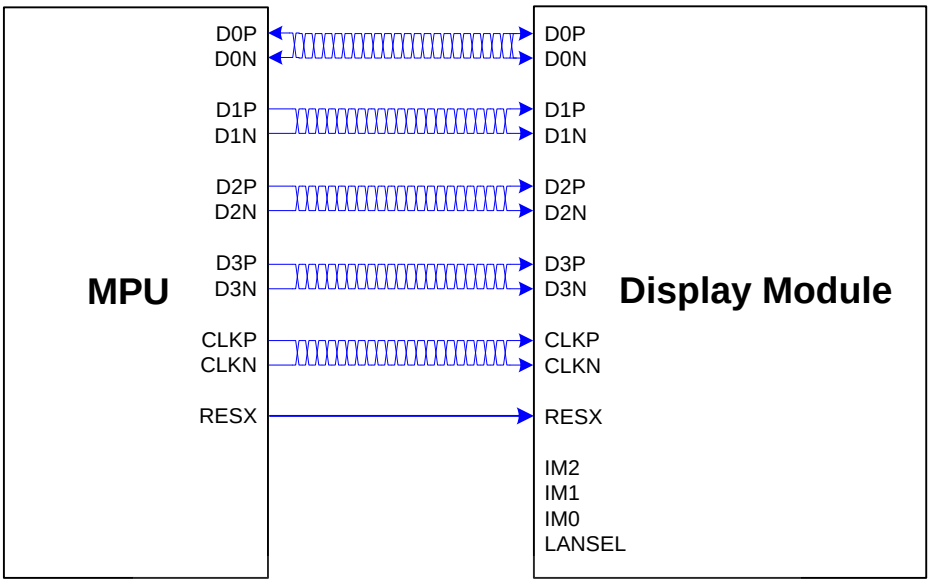


Figure 2: DSI System Interface Diagram

The communication is separated into two different levels between the MCU and the display module:

- Low level communication is done on the interface level.
- High level communication is done on the packet level.

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4.1.2. Interface Level Communication

4.1.2.1. General

The display module uses data and clock lane differential pairs for DSI (DSI-2M). Both differential lane pairs can be driven to Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in the single ended mode, a differential receiver is disable (a termination resistor of the receiver is disable), and it can be driven into a low power mode.

High Speed mode means that differential pairs (the termination resistor of the receiver is enable) are not used in the single ended mode.

Different modes and protocols are used in each mode when transferring information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Table 3: High Speed and Low-Power Lane Pair State Codes

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low Power	
	DATA_P	DATA_N	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential – 0	Note 1	Note1
HS-1	High (HS)	Low (HS)	Differential – 1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS – Request	Mark - 0
LP-10	High (LP)	Low (LP)	Not Defined	LP - Request	Mark - 1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Notes:

1. *Low-Power Receivers (LP-Rx) of the lane pair will check the LP-00 state code when the Lane Pair is in the High Speed (HS) mode.*
2. *If Low-Power Receivers (LP-Rx) of the lane pair recognizes the LP-11 state code, then the lane pair will return to LP-11 of the Control Mode.*
3. *n = 0, 1, 2 and 3 (D1P/N, D2 P/N and D3 P/N lanes only for HS-0 and HS-1)*

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4.1.2.2. DSI CLK Lanes

CLKP/N lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra-Low Power Mode (ULPM) and High Speed Clock Mode (HSCM). Clock lane are in the single ended mode (LP = Low Power) when entering or leaving Low Power Mode (LPM) or Ultra-Low Power Mode (ULPM). Clock lane is in the single ended mode (LP = Low Power) when entering in or leaving High Speed Clock Mode (HSCM).These entering and leaving protocols use Clock lane in the single ended mode to generate an entering or leaving sequence. The principal flow chart of the different Clock lane power modes is illustrated below.

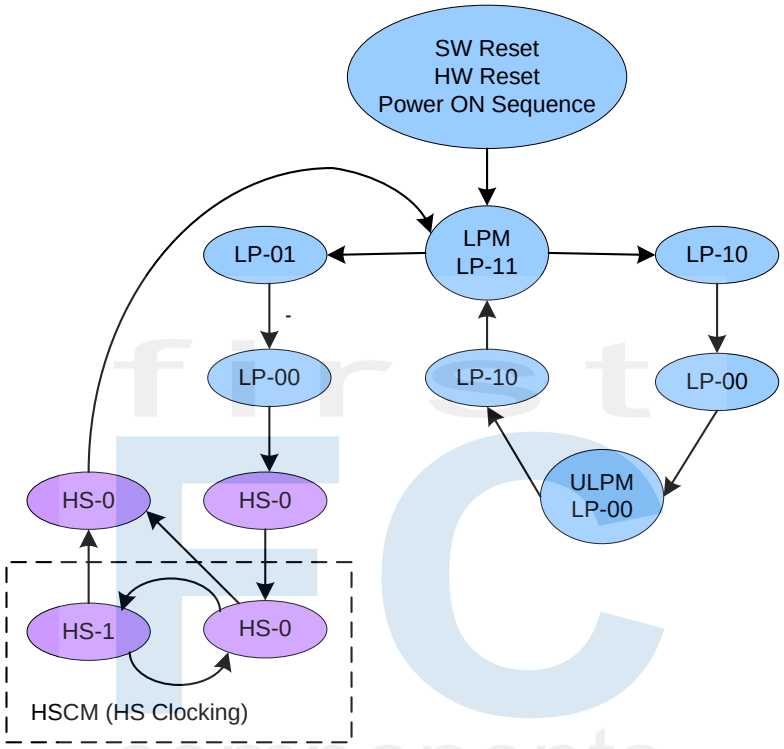


Figure 3: Clock lane Power Modes

4.1.2.2.1. Low Power Mode (LPM)

CLKP/N lanes can be driven to the Low Power Mode (LPM), when CLKP/N lanes enter LP-11 State Code, in three different ways:

1) After SW Reset, HW Reset or Power On Sequence => LP-11

2) After CLKP/N lanes leave Ultra-Low Power Mode (ULPM, LP-00 State Code) => LP-10 => LP-11 (LPM).

This sequence is illustrated below.

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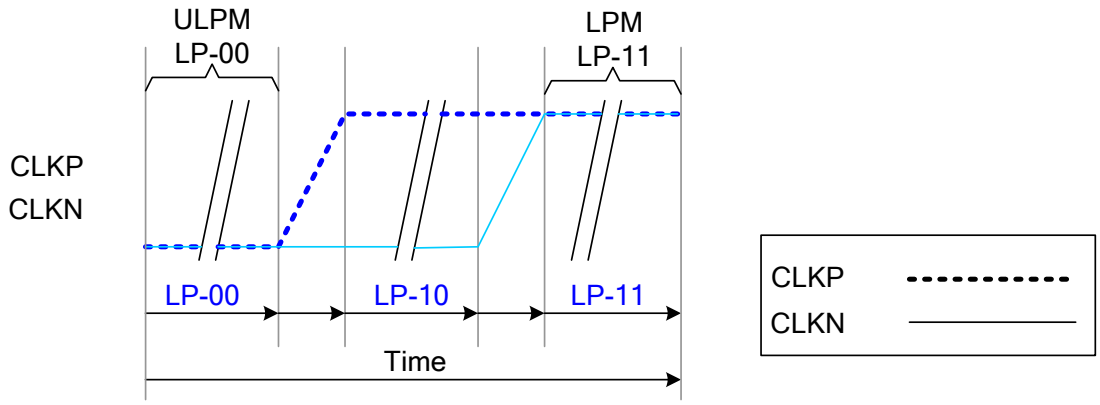


Figure 4: From ULPM to LPM

3) After CLKP/N lanes leave High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) => HS-0=> LP-11 (LPM). This sequence is illustrated below.

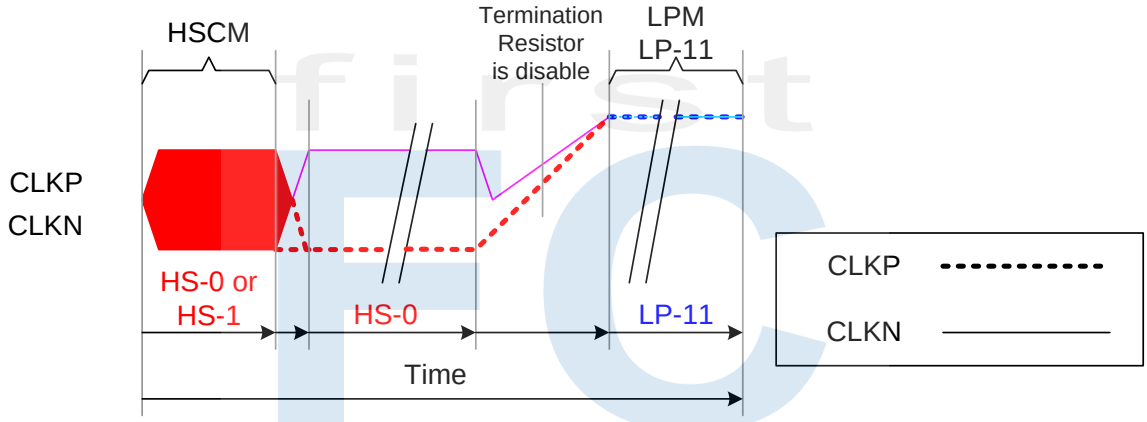


Figure 5: From High Speed Clock Mode (HSCM) to LPM

The changes of all the three modes are illustrated in the flow chart below.

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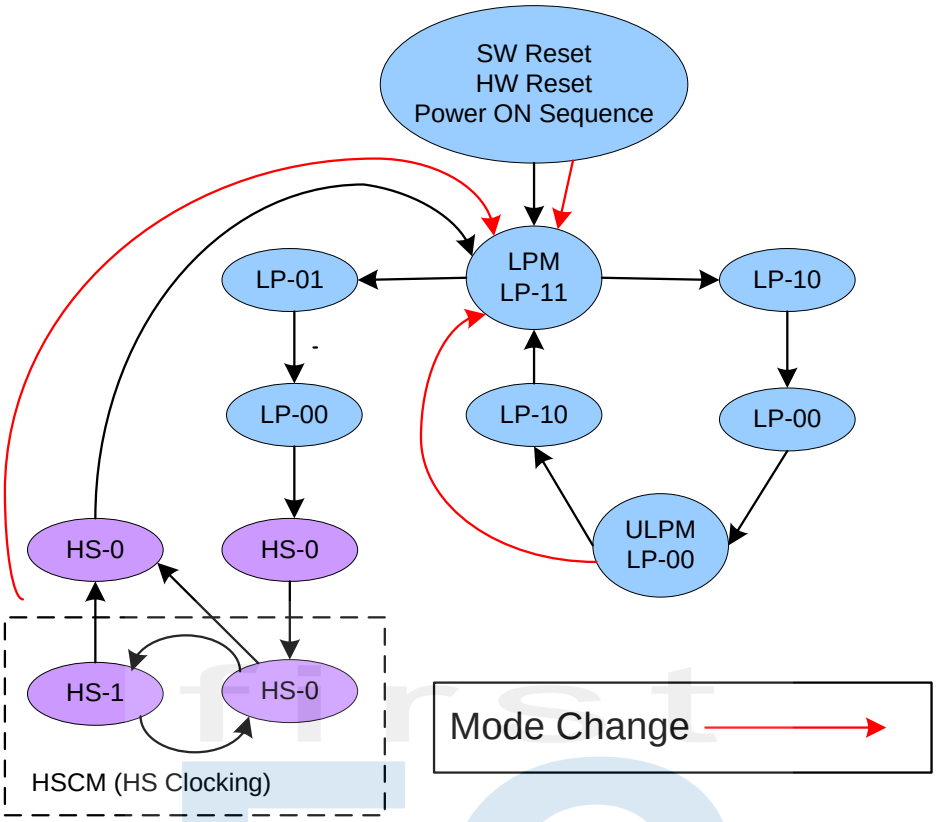


Figure 6: All Three Mode Changes to LPM

4.1.2.2.2. Ultra-Low Power Mode (ULPM)

CLKP/N lanes can be driven to the Ultra-Low power Mode (ULPM) when CLK lanes enter the LP-00 State Code. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-10 => LP-00 (ULPM). This sequence is illustrated below.

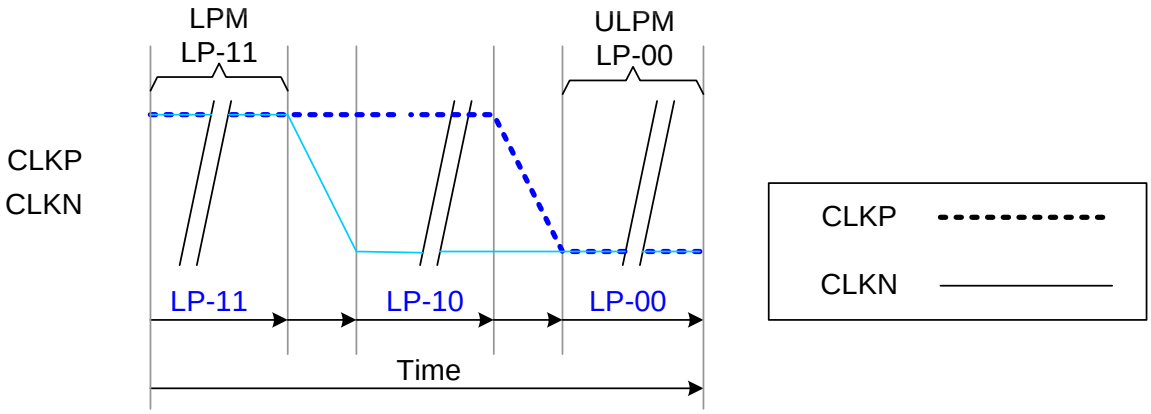


Figure 7: From LPM to ULPM

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The mode change is also illustrated below.

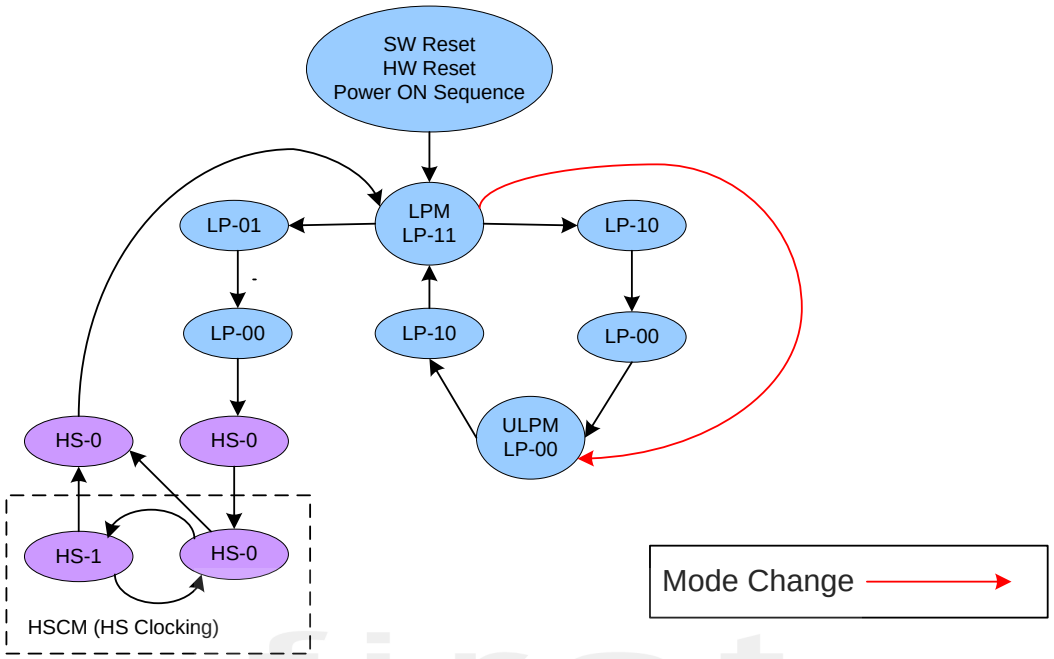


Figure 8: Mode Change from LPM to ULPM

4.1.2.2.3. High-Speed Clock Mode (HSCM)

CLKP/N lanes can be driven to the High Speed Clock Mode (HSCM) when CLK lanes start to function between HS-0 and HS-1 State Codes. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-01 => LP-00 => HS-0 => HS-0/1 (HSCM). This sequence is illustrated below.

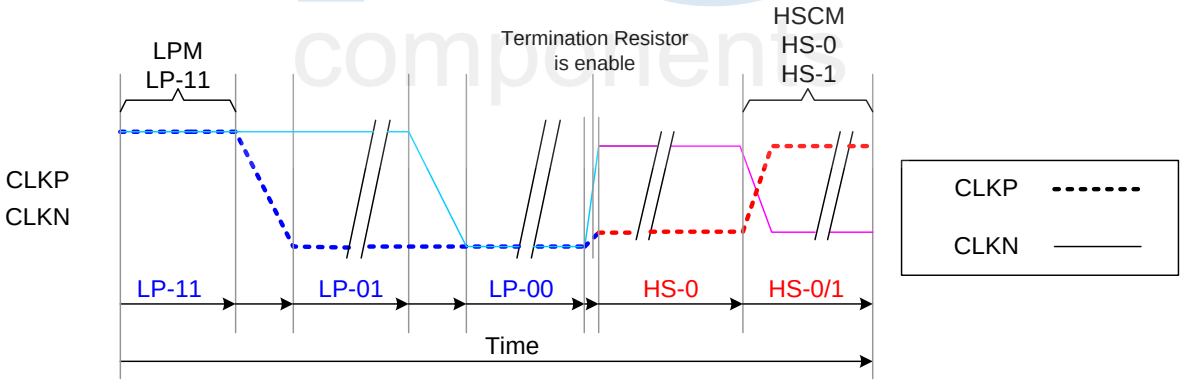


Figure 9: From LPM to HSCM

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The mode change is also illustrated below.

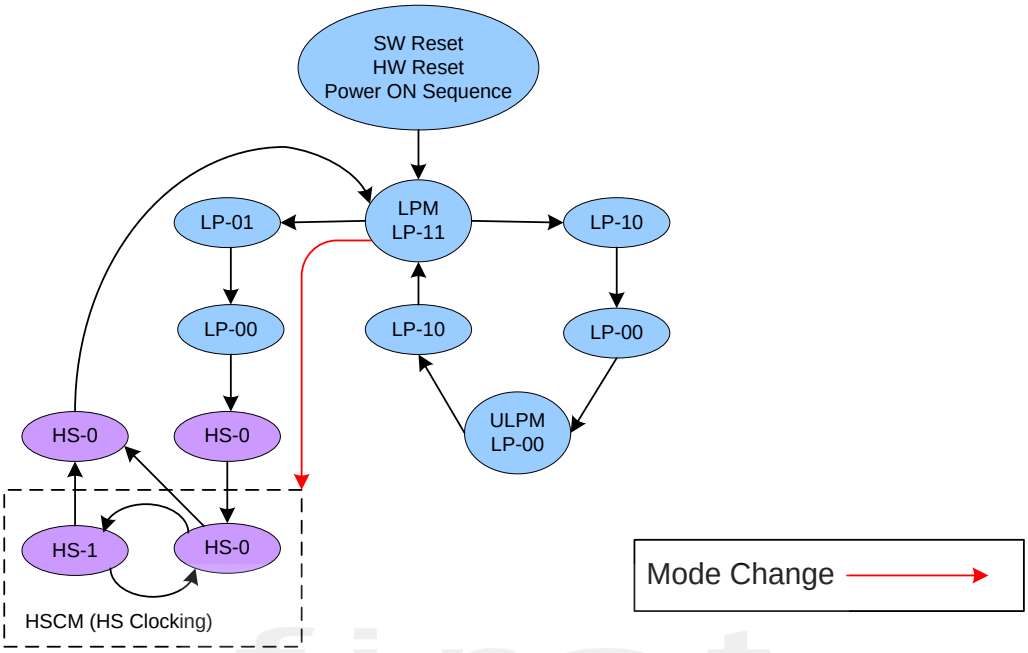


Figure 10: Mode Change from LPM to HSCM

The high speed clock (CLKP/N) starts before high speed data is sent via data lanes. The high speed clock continues clocking after the high speed data sending is stopped.

The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0

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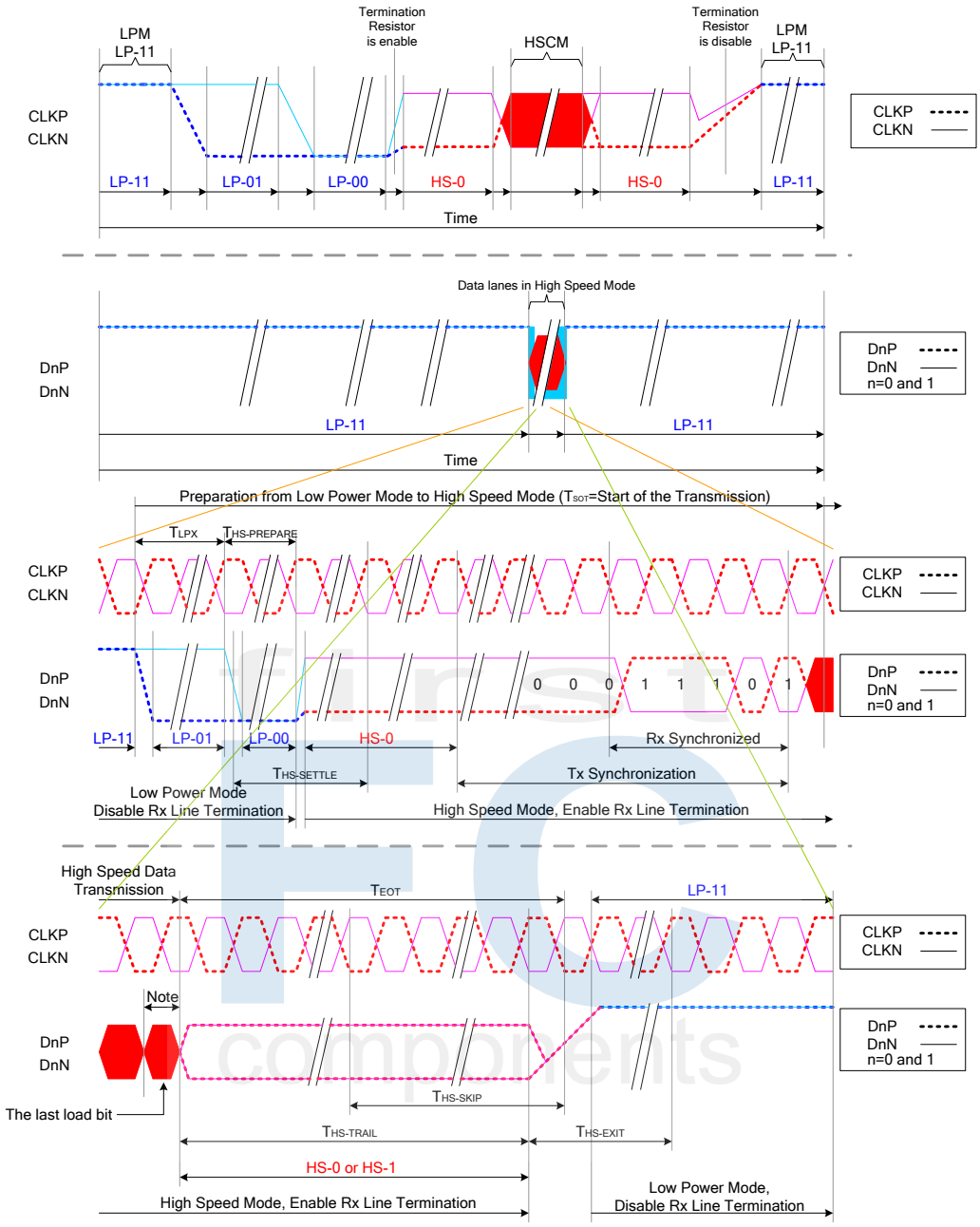


Figure 11: High Speed Clock Burst

Notes:

1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

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4.1.2.3. DSI Data Lanes

4.1.2.3.1. General

D3P/N, D2P/N, D1P/N and D0P/N Data Lanes can be driven into different modes:

- Escape Mode (Only D0P/N data lane is used)
- High-Speed Data Transmission (all data lanes are used)
- Bus Turnaround Request (Only D0P/N data lane are used)

These modes and their entering codes are defined in the following table.

Table 4: Entering and Leaving Sequences

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode[1]	LP-11 → LP-10 → LP-00 → LP-01 → LP-00	LP-00 → LP-10 → LP-11 (Mark-1)
High-Speed Data Transmission[2]	LP-11 → LP-01 → LP-00 → HS-0	(HS-0 or HS-1) → LP-11
Bus Turnaround Request[3]	LP-11 → LP-10 → LP-00 → LP-10 → LP-00	Hi-Z

4.1.2.3.2. Escape Modes

D0P/N data lanes can be used in different Escape Modes when data lanes are in the Low Power (LP) mode. These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) from the MCU to the display module,
- Drive data lanes to “Ultra-Low Power State” (ULPS),
- Indicate “Remote Application Reset” (RAR), which can reset the display module,
- Indicate “Acknowledge” (ACK), which is used to transmit a non-error event from the display module to the MCU.

The basic sequence of the Escape Mode is as follows:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Escape Command (EC), which is coded, when one of the data lanes changes from low-to-high-to-low then this changed data lane presents the value of the current data bit (D0P = 1, D0N= 0). When DSI-D0 changes from low-to-high-to-low, the receiver will latch a data bit, which value is logical 0. The receiver will use this low-to-high-to-low transition as its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 => LP-10 => LP-11
- End: LP-11

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This basic construction is illustrated below:

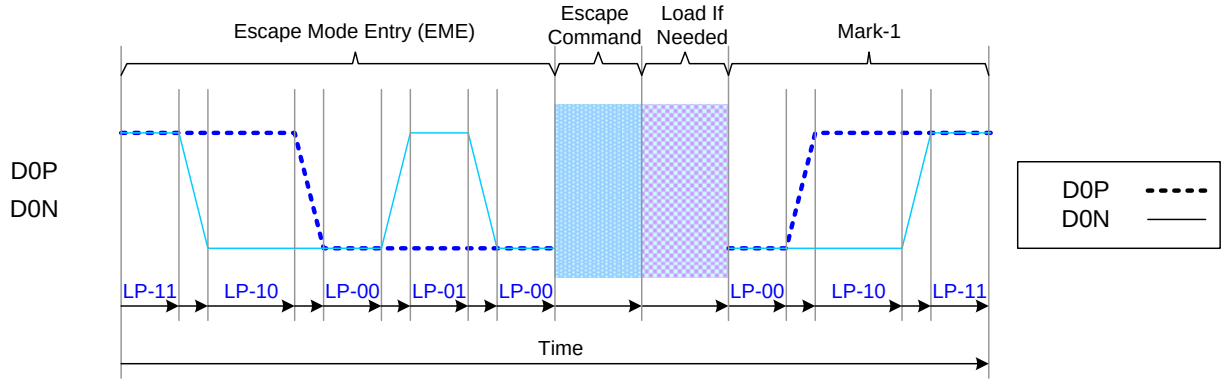


Figure 12 General Escape Mode Sequence

A total of eight Escape Commands (EC) are divided into two types: Mode and Trigger, as shown in Table 5: Escape Commands.

An example of the Mode type Escape Command is 'Ultra-Low Power Mode', where the MCU instructs the display module to enter its Ultra-Low Power Mode.

Escape commands are defined in the following table.

Table 5: Escape Commands

Escape command	Command Type Mode/Trigger	Entry command Pattern (First Bit → Last Bit Transmitted)	Dn	D0
Low-Power Data Transmission	Mode	1110 0001 b	-	X
Ultra-Low Power Mode	Mode	0001 1110 b	X	X
Undefined-1, Note 1	Mode	1001 1111 b	-	-
Undefined-2, Note 1	Mode	1101 1110 b	-	-
Remote Application Reset	Trigger	0110 0010 b	-	X
Acknowledge	Trigger	0010 0001 b	-	X
Unknown-5, Note 1	Trigger	1010 0000 b	-	-

Notes:

1. This Escape command support is not implemented on the display module.

2. n = 1

3. x = Supported

4. - = Not Supported

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4.1.2.3.2.1. Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in the Low-Power Data Transmission (LPDT) mode when data lanes enter the Escape Mode and Low-Power Data Transmission (LPDT) command is sent to the display module. The display module also uses the same sequence when it sends data to the MCU. The Low Power Data Transmission (LPDT) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Low-Power Data Transmission (LPDT) command in the Escape Mode: 1110 0001 (first to last bit)
- Load (Data):
  - ✧ One or more bytes (one byte = 8 bit)
  - ✧ Data lanes are in pause mode when data lanes are stopped (both lanes are low) between bytes
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

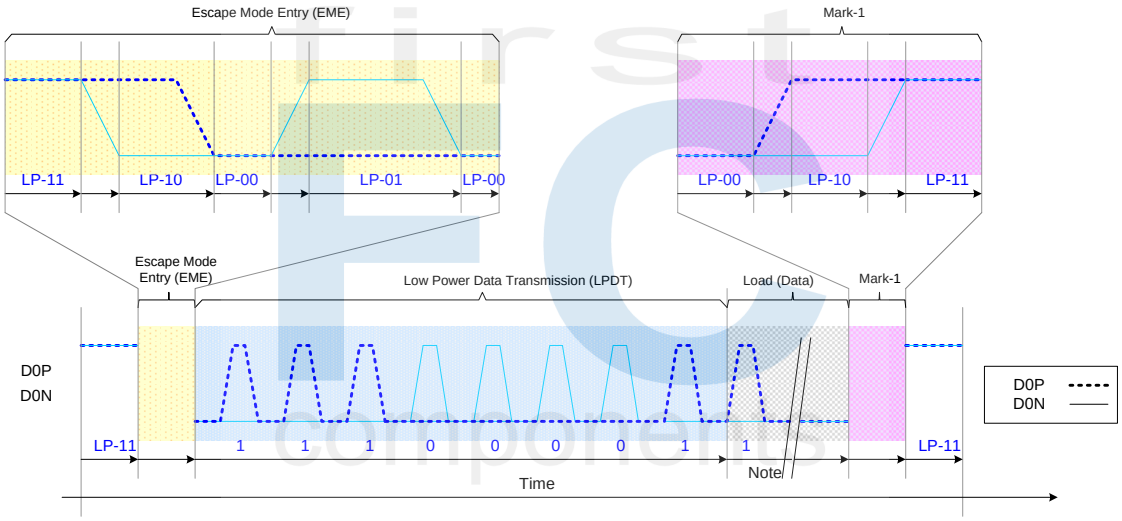


Figure 13: Low-Power Data Transmission (LPDT)

Note: *Load (Data) presents that the first bit is the logical 1 in this example.*

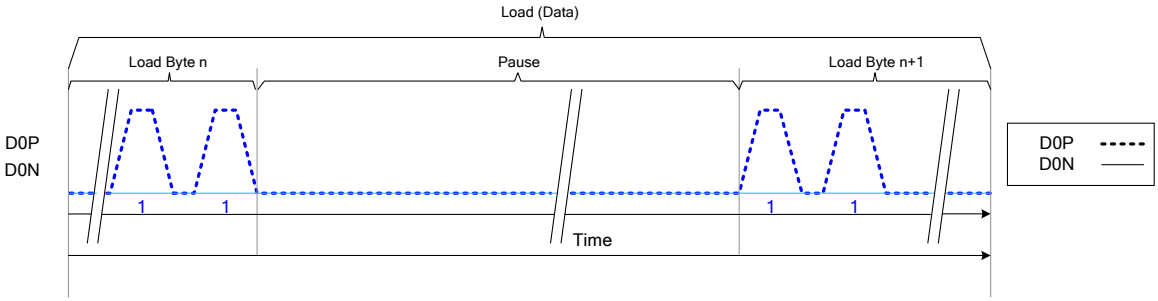


Figure 14: Pause (Example)

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4.1.2.3.2.2. Ultra-Low Power State (ULPS)

The MCU can force data lanes get into the Ultra-Low Power State (ULPS) mode when data lanes enter the Escape Mode. The Ultra-Low Power State (ULPS) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Ultra-Low Power State (ULPS) command in the Escape Mode: 0001 1110 (first to last bit)
- Ultra-Low Power State (ULPS) when the MCU keeps data lanes low
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11 (Next command must wait 100us after data lanes leave ULPS)

This sequence is illustrated for reference purposes below:

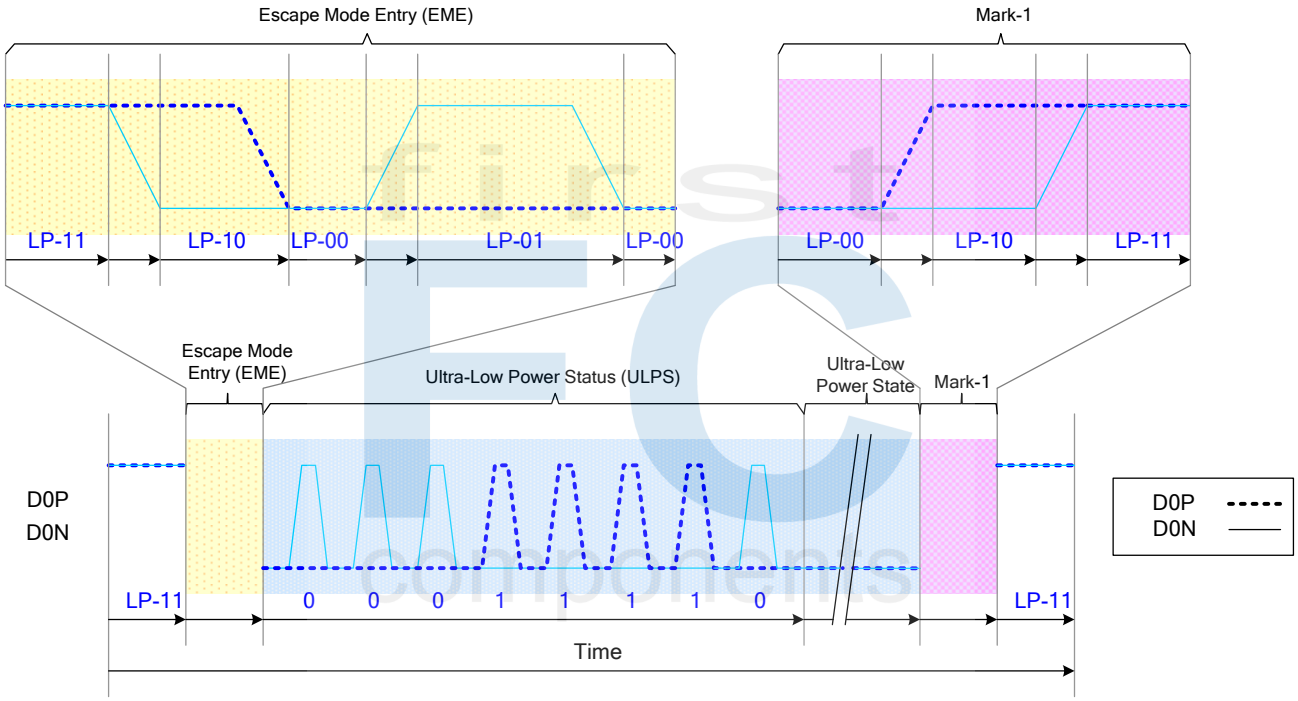


Figure 15: Ultra-Low Power State (ULPS)

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4.1.2.3.2.3. Remote Application Reset (RAR)

The MCU can inform the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes enter the Escape Mode. The Remote Application Reset (RAR) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

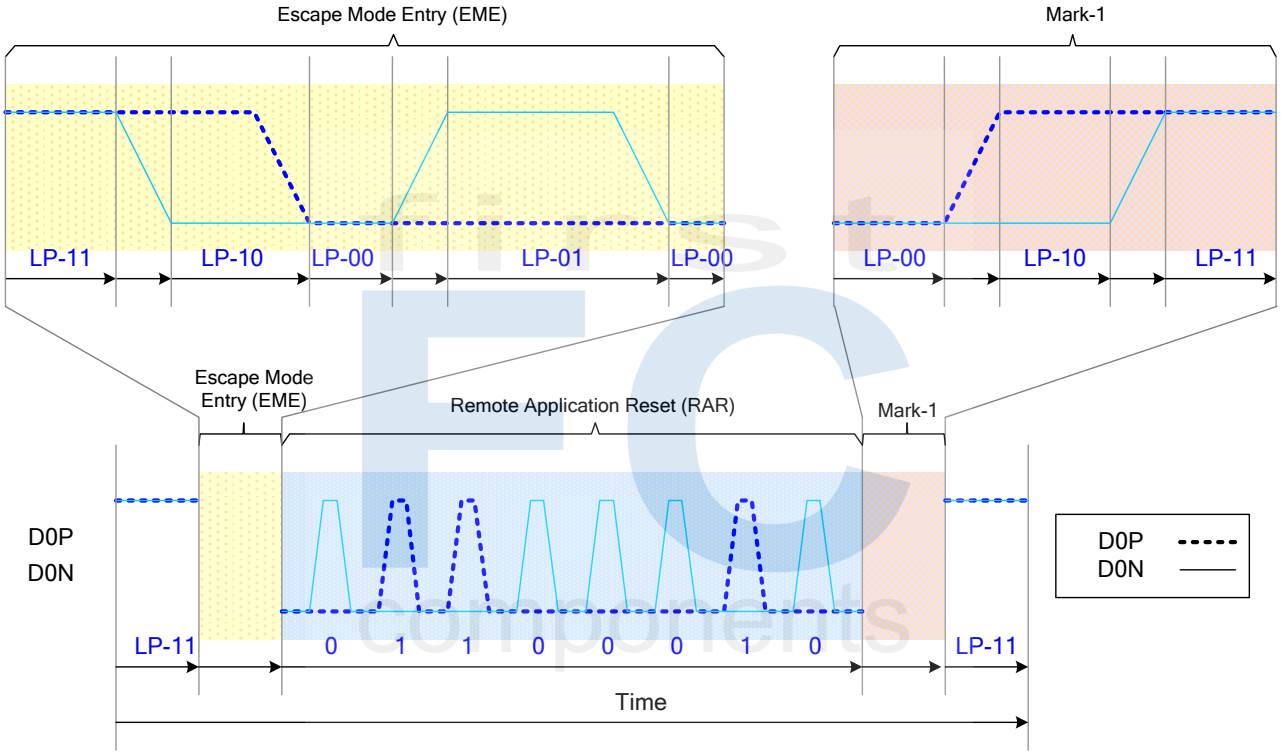


Figure 16: Remote Application Reset (RAR)

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4.1.2.3.2.4. Acknowledge (ACK)

The display module can inform the MCU an error is not recognized by Acknowledge (ACK). The display module sends the Acknowledge (ACK) with the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Acknowledge (ACK) command in the Escape Mode: 0010 0001 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

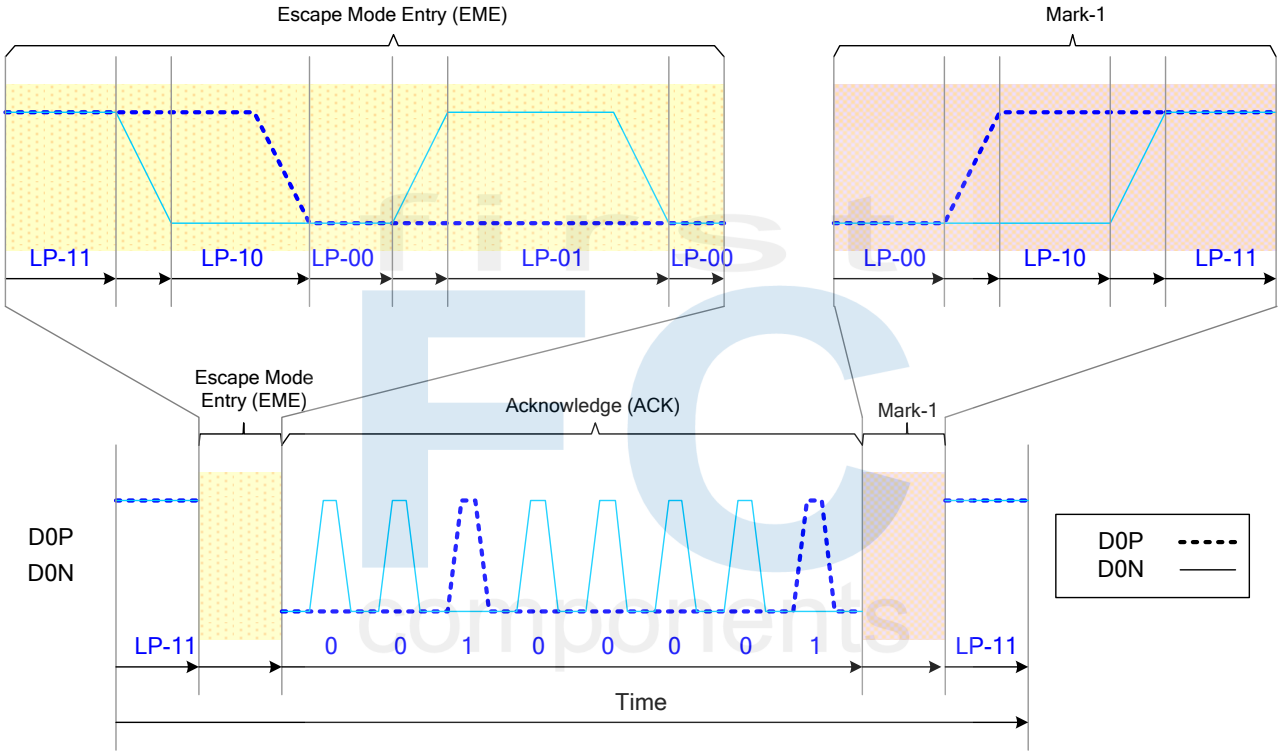


Figure 17: Acknowledge (ACK)

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4.1.2.3.3. High-Speed Data Transmission (HSDT)

4.1.2.3.3.1. Entering High-Speed Data Transmission (TSOT of HSDT)

The display module enters High-Speed Data Transmission (HSDT) when Clock lane CLKP/N have already entered the High-Speed Clock Mode (HSCM) by the MCU. See more information in the section “4.1.2.2.3 High-Speed Clock Mode (HSCM)”.

Data lanes D3P/N, D2P/N, D1P/N and D0P/N of the display module enter the High-Speed Data Transmission (TSOT of HSDT) as follows:

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

The sequence of entering High-Speed Data Transmission (TSOT of HSDT) is illustrated below:

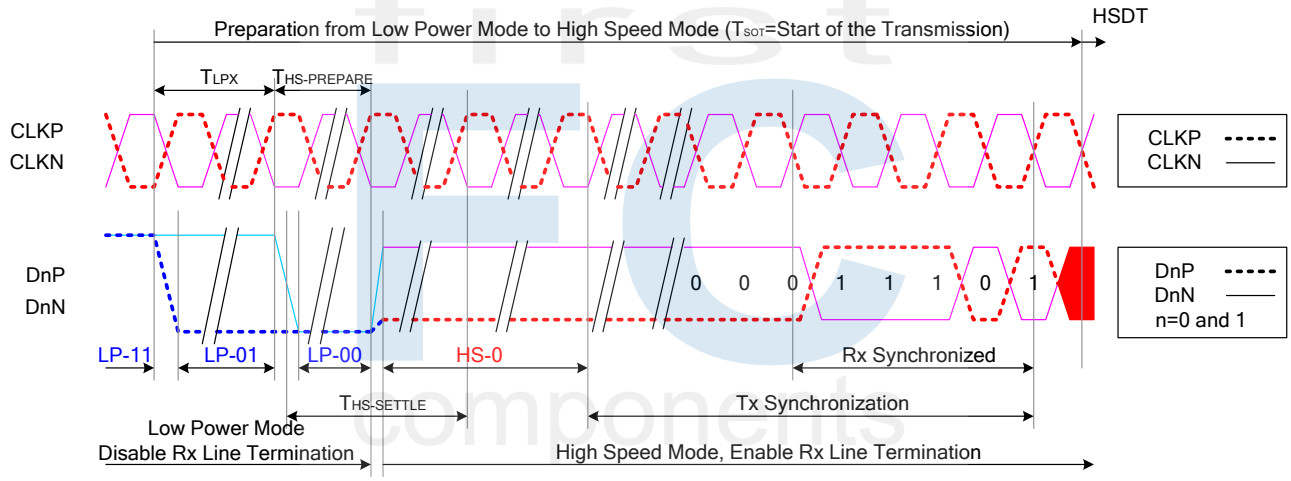


Figure 18: Entering High-Speed Data Transmission (TSOT of HSDT)

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4.1.2.3.3.2. Leaving High-Speed Data Transmission (TEOT of HSDT)

The display module leaves the High-Speed Data Transmission (TEOT of HSDT) when Clock lane DSICLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU, and this HSCM is kept until data lanes D3P/N, D2P/N, D1P/N and D0P/N are in the LP-11 mode. See more information in the section “4.1.2.2.3 High-Speed Clock Mode (HSCM)”. Data lanes D3P/N, D2P/N, D1P/N and D0P/N of the display module leave the High-Speed Data Transmission (TEOT of HSDT) as follows:

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
  - ✧ MCU changes to HS-1, if the last load bit is HS-0
  - ✧ MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

The sequence of leaving High-Speed Data Transmission (TEOT of HSDT) is illustrated below:

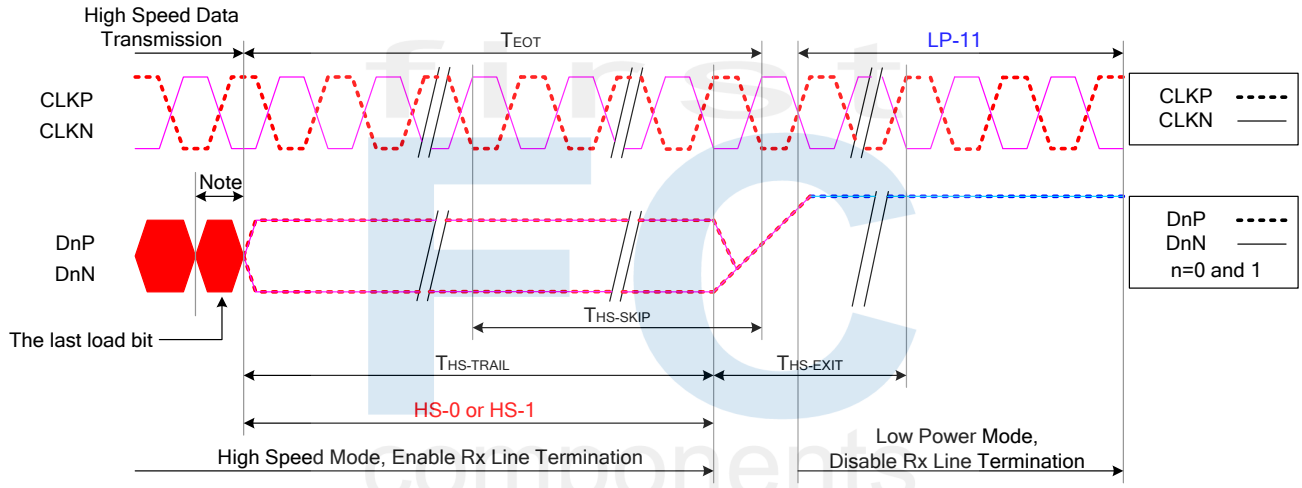


Figure 19: Leaving High-Speed Data Transmission (TEOT of HSDT)

Notes:

1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

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4.1.2.3.3.3. Burst of the High-Speed Data Transmission (HSDT)

The burst of the “High-Speed Data Transmission” (HSDT) can consist of one or several data packet(s). These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined in the section “4.1.3.1 Short Packet (SPa) and Long Packet (LPa) Structures”. These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

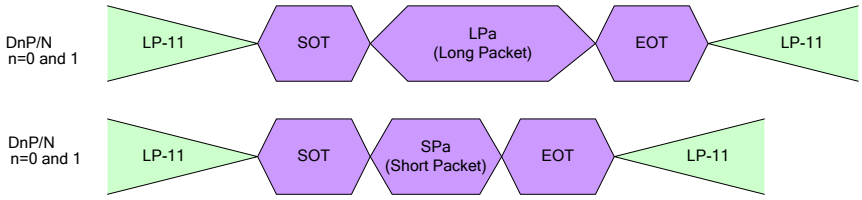


Figure 20: Single Packet in High-Speed Data Transmissions

The multiple packets in High-Speed Data Transmission are illustrated for reference purposes below:

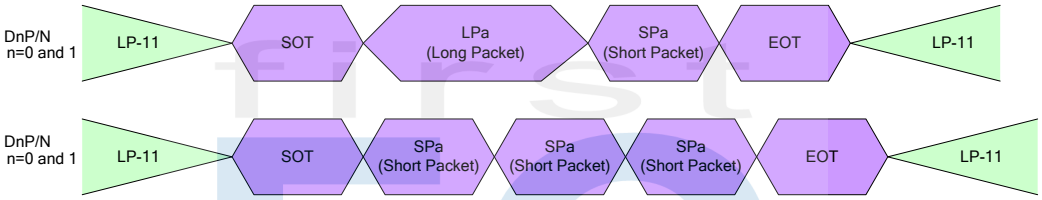


Figure 21: Multiple Packets in High-Speed Data Transmission – Examples

Table 6: Abbreviations

Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Both of Data lanes are ‘1’s (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

Byte orders of the sent packet in High-Speed Data Transmission (HSDT) are as follows.

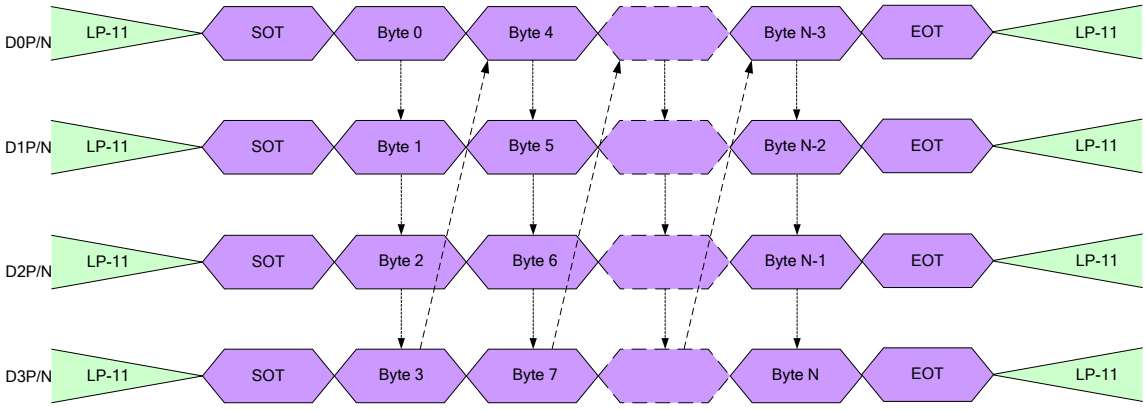


Figure 22: Number of Bytes, N, transmitted is an integer multiple of the number of lanes

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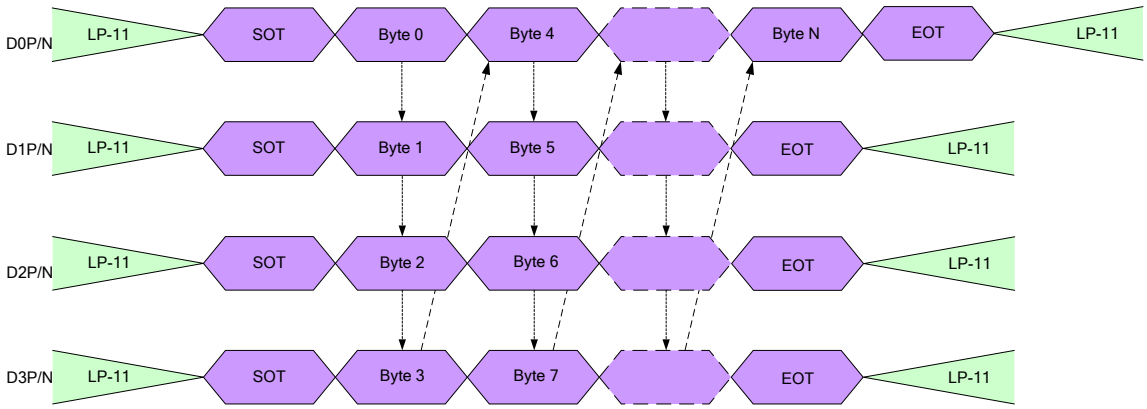


Figure 23: Number of Bytes, N, transmitted is NOT an integer multiple of the number of lanes (Example 1)

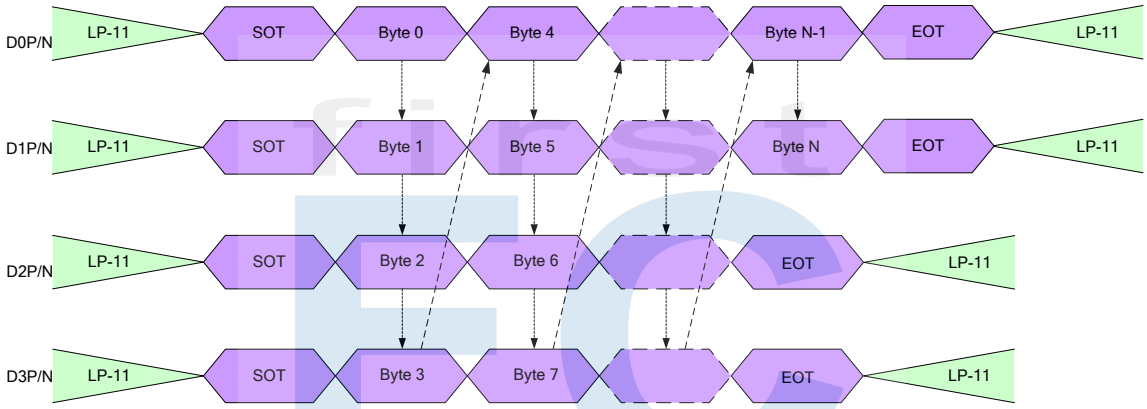


Figure 24: Number of Bytes, N, transmitted is NOT an integer multiple of the number of lanes (Example 2)

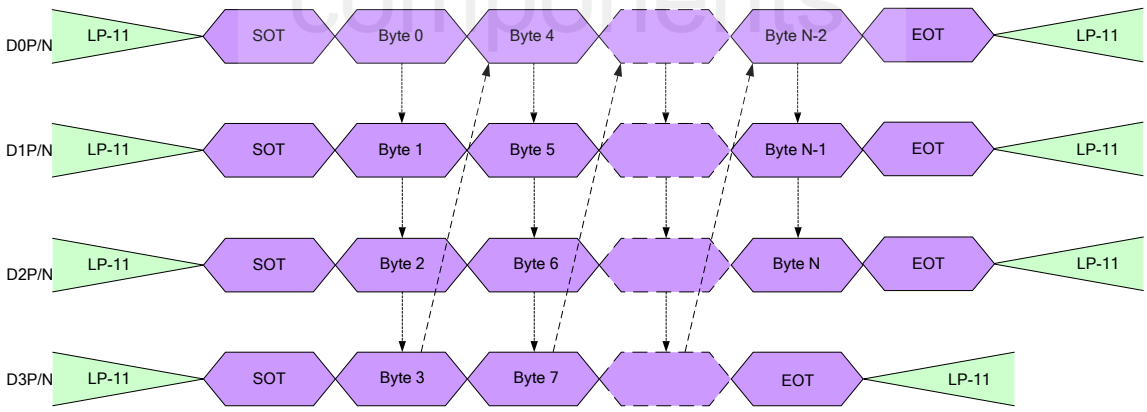


Figure 25: Number of Bytes, N, transmitted is NOT an integer multiple of the number of lanes (Example 3)

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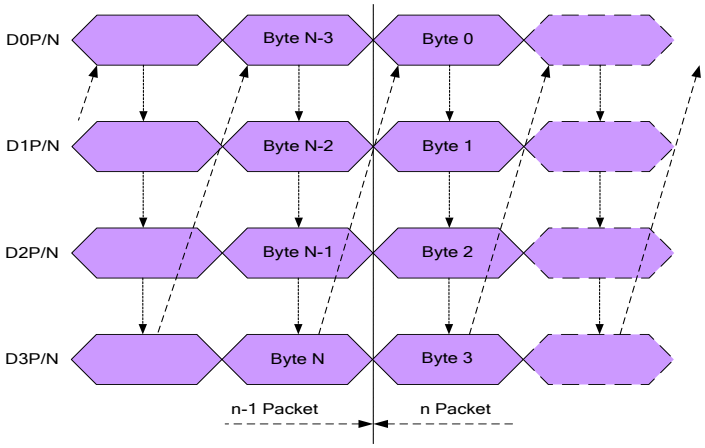


Figure 26: Continuous Multiple Packets in HSDT when Number of Bytes is Equal on Data Lanes at the End of the Packet

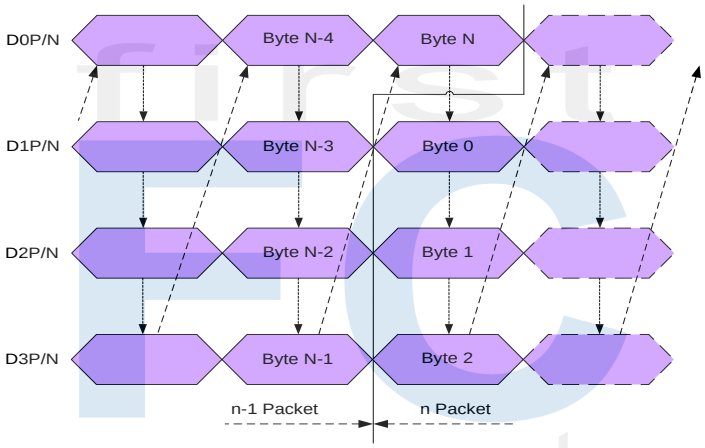


Figure 27: Continuous Multiple Packets in HSDT when Number of Bytes is not Equal on Data Lanes at the End of the Packet (Example 1)

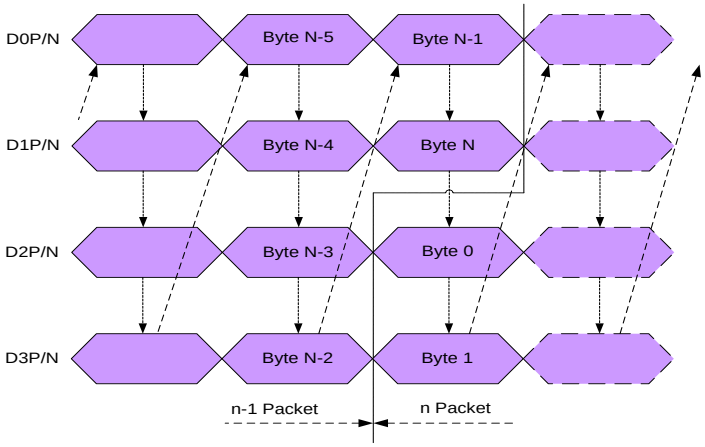


Figure 28: Continuous Multiple Packets in HSDT when Number of Bytes is not Equal on Data Lanes at the End of the Packet (Example 2)

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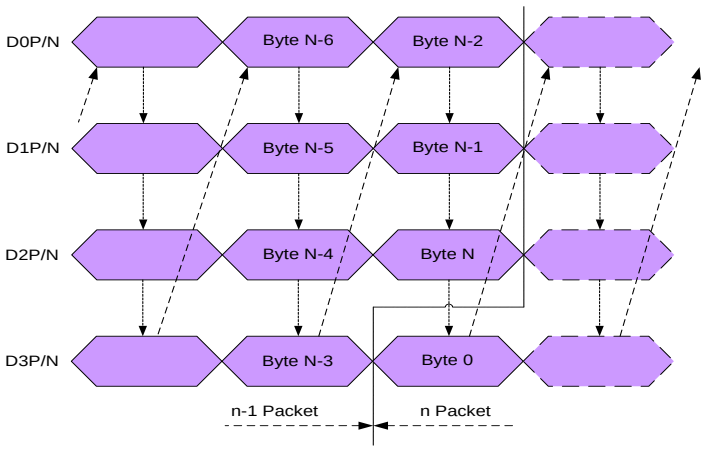


Figure 29: Continuous Multiple Packets in HSDT when Number of Bytes is not Equal on Data Lanes at the End of the Packet (Example 3)

first FC components

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4.1.2.3.4. Bus Turnaround (BTA)

The MCU or display module, which controls D0P/N Data Lanes, can start a bus turnaround procedure when it requires information from a receiver, which can be the MCU or display module.

The MCU and display module use the same sequence when this bus turnaround procedure is used. The sequence, when the MCU wants to do the bus turnaround procedure to the display module, is described for reference purposes as follows:

- Start (MCU): LP-11
- Turnaround Request (MCU): LP-11 => LP-10 => LP-00 => LP-10 => LP-00
- The MCU waits until the display module starts to control D0P/N data lanes and the MCU stops to control D0P/N data lanes (= High-Z)
- The display module changes to the stop mode: LP-00 => LP-10 => LP-11

The bus turnaround procedure (from the MCU to the display module) is illustrated below:

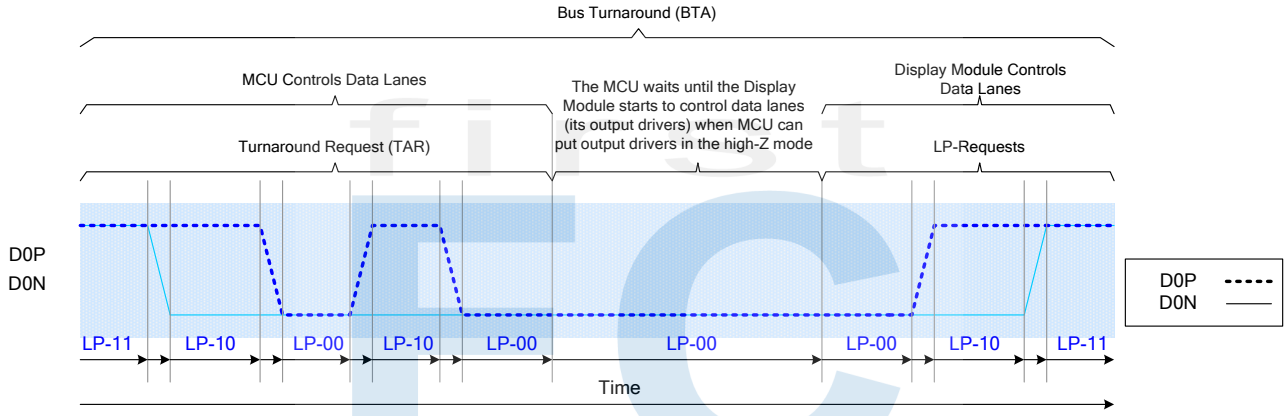


Figure 30: Bus Turnaround Procedure

MCU and display module terms can be switched in Figure 30 if the Bus Turnaround (BTA) is from the display module to the MCU.

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4.1.3. Packet Level Communication

4.1.3.1. Short Packet (SPa) and Long Packet (LPa) Structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes. The lengths of the packets are:

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

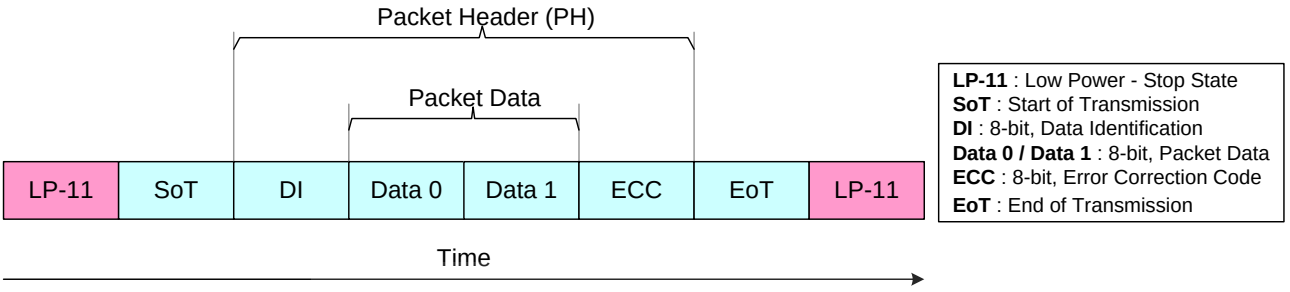


Figure 31: Short Packet (SPa) Structure

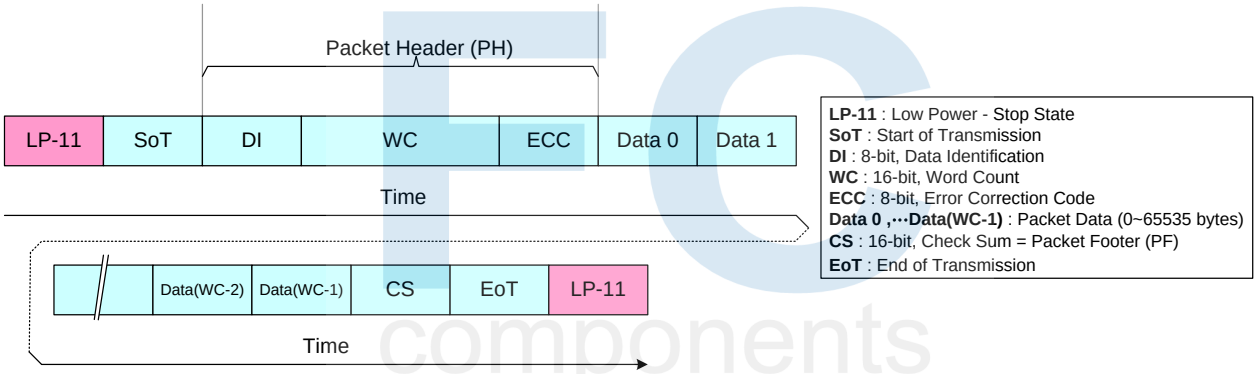


Figure 32: Long Packet (LPa) Structure

Notes:

1. *Figure 31 and Figure 32 present a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).*
2. *The other possibility is that SoT, EoT and LP-11 are not needed between packets if packets are sent in multiple packet format, e.g.*
   - *LP-11 => SoT => SPa => LPa => SPa => SPa => EoT => LP-11*
   - *LP-11 => SoT => SPa => SPa => SPa => EoT => LP-11*
   - *LP-11 => SoT => LPa => LPa => LPa => EoT => LP-11*

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4.1.3.1.1. Bit Order of the Byte on Packets

The bit order of the byte, what is used in packets, is that the Least Significant Bit (LSB) of the byte is sent first, and the Most Significant Bit (MSB) is sent last. The order is illustrated for reference purposes below.

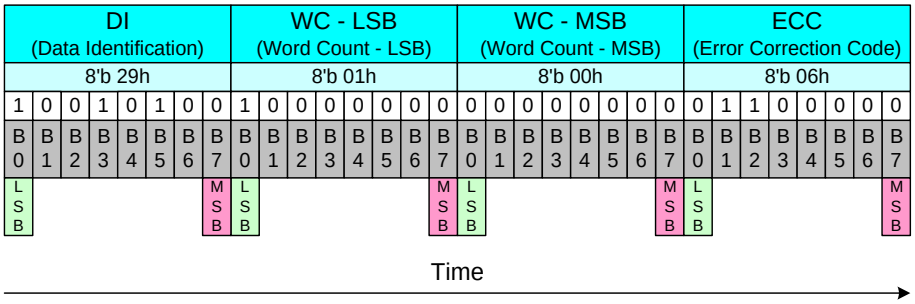


Figure 33: Bit Order of the Byte on Packets

4.1.3.1.2. Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used in packets, is that the Least Significant (LS) Byte of the information is sent first and the Most Significant (MS) Byte is sent last. For example, Word Count (WC) consists of 2 bytes (= 16 bits); while the LS byte is sent first and the MS byte is sent last. The order is illustrated for reference purposes below.

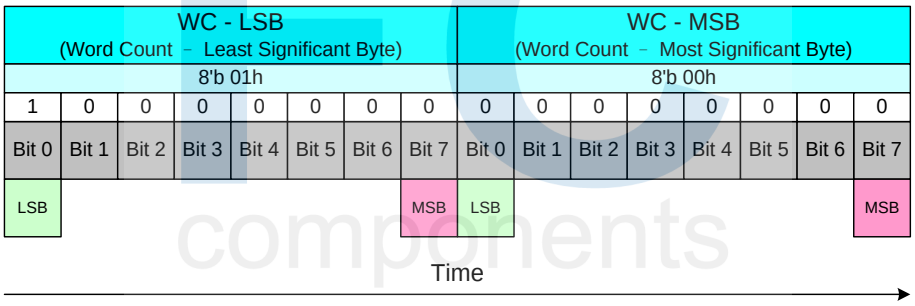


Figure 34: Byte Order of the Multiple Byte Information on Packets

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4.1.3.1.3. Packet Header (PH)

The packet header always consists of 4 bytes. The content of these 4 bytes are different for Short Packet (SPa) and Long Packet (LPa).

Short Packet (SPa):

- 1st byte: Data Identification (DI) => Identify that this is a Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)

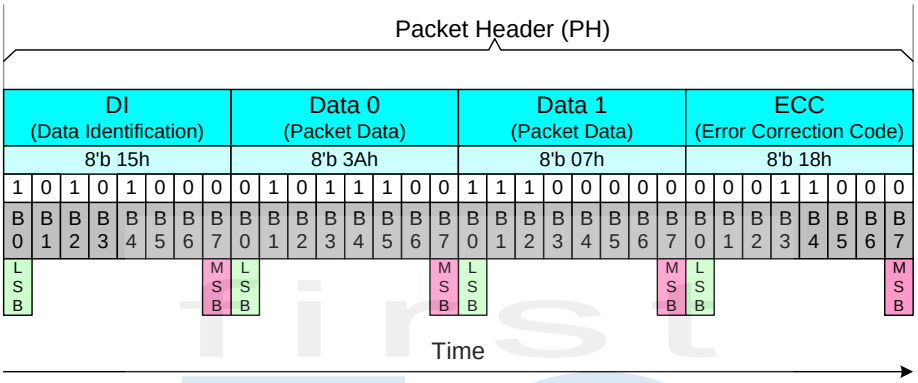


Figure 35: Packet Header (PH) in a Short Packet (SPa)

Long Packet (LPa):

- 1st byte: Data Identification (DI) => Identify that this is a Long Packet (LPa)
- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)

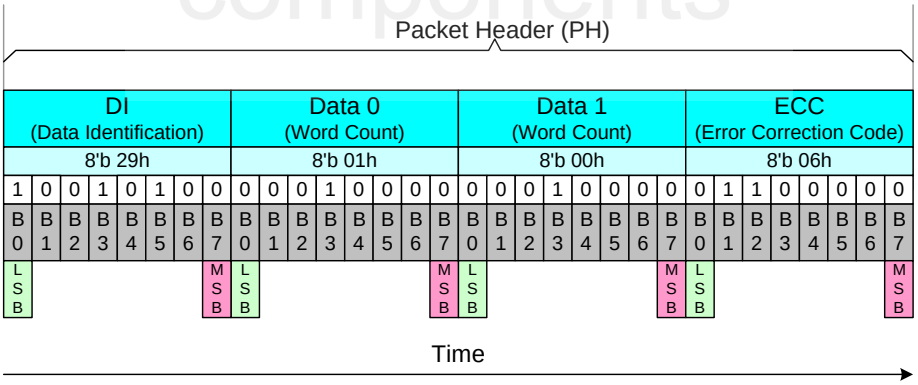


Figure 36: Packet Header (PH) in a Long Packet (LPa)

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4.1.3.1.3.1. Data Identification (DI)

Data Identification (DI) is a part of the Packet Header (PH), and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI [7...6]
- Data Type (DT), 6 bits, DI [5…0]

The Data Identification (DI) structure is illustrated, see the figure below.

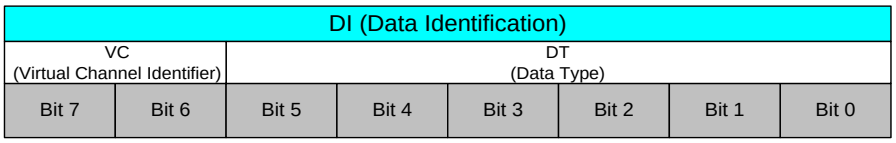


Figure 37: Data Identification (DI) Structure

Data Identification (DI) in the Packet Header (PH) is illustrated for reference purposes below.

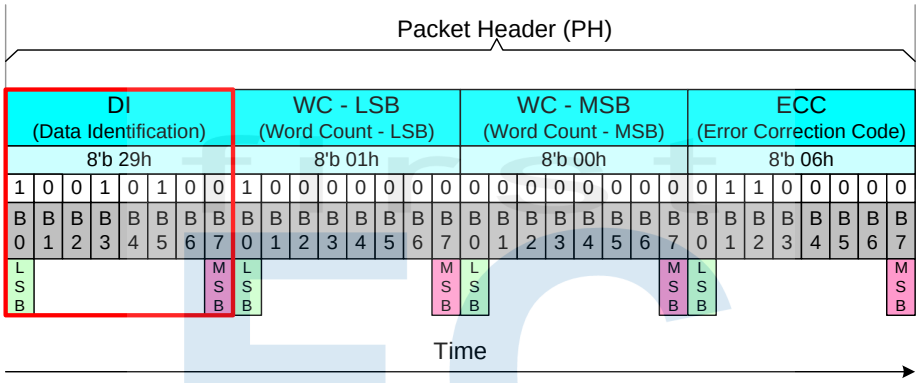


Figure 38: Data Identification (DI) on the Packet Header (PH)

4.1.3.1.3.1.1. Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI [7…6]) structure, and it is used to address where a packet is to be sent from the MCU. Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

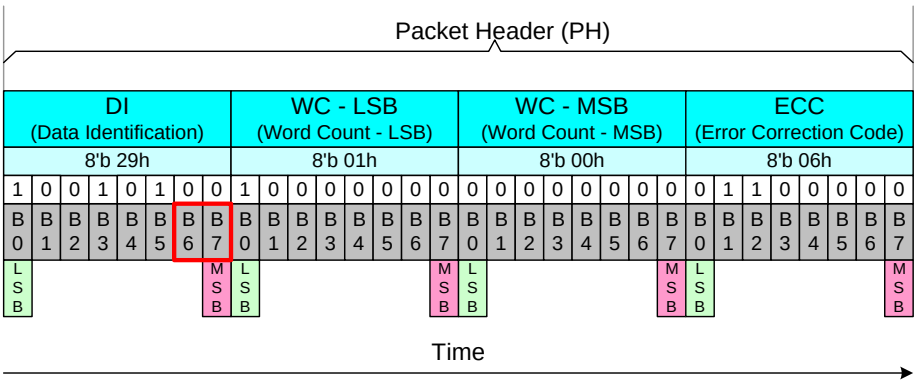


Figure 39: Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can assign 4 different channels for 4 different display modules. Devices will use the same virtual channel as which the MCU uses to send packets to them, e.g.

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- The MCU uses the virtual channel 0 when it sends packets to the ILI9881C-0D
- The ILI9881C-0D also uses the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.

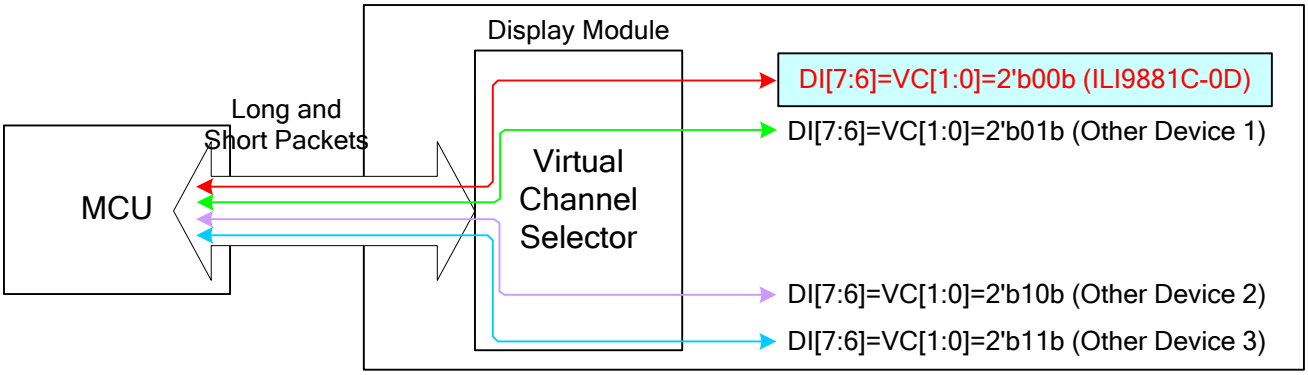


Figure 40: Virtual Channel (VC) Configuration

Virtual Channel (VC) is always 0 (DI [7..6] = VC [1..0] = 00b) when the MCU sends “End of Transmission Packet” to the display module. See the section “4.1.3.2.1.7 End of Transmission Packet (EoTP)”.

This display module does not support the virtual channel selector for other devices (1 to 3) when the only possible virtual channel (VC [1..0]) is 00b for the ILI9881C-0D.

4.1.3.1.3.1.2. Data Type (DT)

Data Type (DT) is a part of Data Identification (DI [5…0]) structure, and it is used to define the type of the used data in a packet. Bits of the Data Type (DT) are illustrated for reference purposes below.

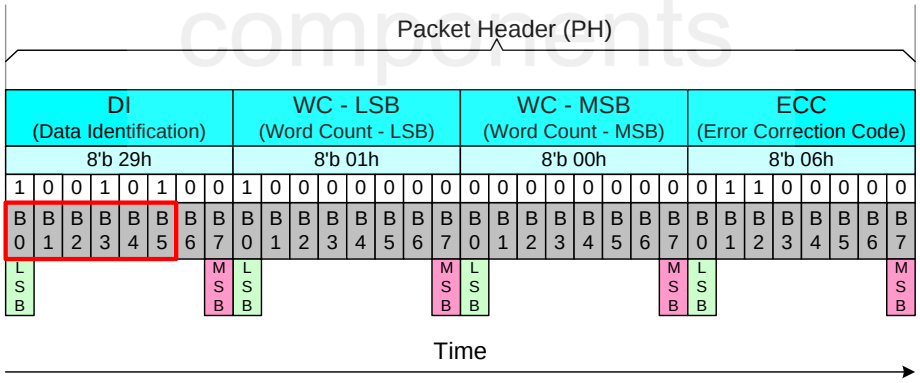


Figure 41: Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines the used packet is a Short Packet (SPa) or a Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. These Data Types (DT) are defined in the tables below.

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Table 7: Data Type (DT) from the MCU to the Display Module

From the MCU to the Display Module								
Bit5	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Hex**	**Description**	**Short/Long Packet**
0	0	0	0	0	1	01	Sync Event, V Sync Start	SPa (Short Packet)
0	1	0	0	0	1	11	Sync Event, V Sync End	SPa (Short Packet)
1	0	0	0	0	1	21	Sync Event, H Sync Start	SPa (Short Packet)
1	1	0	0	0	1	31	Sync Event, H Sync End	SPa (Short Packet)
0	0	1	0	0	0	08	End of Transmission Packet (EoTP) Note1	SPa (Short Packet)
0	0	0	0	1	0	02	Color Mode Off Command	SPa (Short Packet)
0	1	0	0	1	0	12	Color Mode On Command	SPa (Short Packet)
1	0	0	0	1	0	22	Shut Down Peripheral Command	SPa (Short Packet)
1	1	0	0	1	0	32	Turn On Peripheral Command	SPa (Short Packet)
0	0	0	0	1	1	03	Generic Short WRITE, no parameters	SPa (Short Packet)
0	1	0	0	1	1	13	Generic Short WRITE, 1 parameters	SPa (Short Packet)
1	0	0	0	1	1	23	Generic Short WRITE, 2 parameters	SPa (Short Packet)
0	0	0	1	0	0	04	Generic Short READ, no parameters	SPa (Short Packet)
0	1	0	1	0	0	14	Generic Short READ, 1 parameters	SPa (Short Packet)
1	0	0	1	0	0	24	Generic Short READ, 2 parameters	SPa (Short Packet)
0	0	0	1	0	1	05	DCS Write, No Parameter	SPa (Short Packet)
0	1	0	1	0	1	15	DCS Write, 1 Parameter	SPa (Short Packet)
0	0	0	1	1	0	06	DCS Read, No Parameter	SPa (Short Packet)
1	1	0	1	1	1	37	Set Maximum Return Packet Size	SPa (Short Packet)
0	0	1	0	0	1	09	Null Packet, No Data, Note2	LPa (Long Packet)
0	1	1	0	0	1	19	Blanking Packet, no data	LPa (Long Packet)
1	0	1	0	0	1	29	Generic Long Write	LPa (Long Packet)
1	1	1	0	0	1	39	DCS Write Long	LPa (Long Packet)
0	0	1	1	1	0	0E	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	LPa (Long Packet)
0	1	1	1	1	0	1E	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	LPa (Long Packet)
1	0	1	1	1	0	2E	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	LPa (Long Packet)
1	1	1	1	1	0	3E	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	LPa (Long Packet)
x	x	0	0	0	0	x0	DO NOT USE	
x	x	1	1	1	1	xF	All unspecified codes are reserved	

Notes:

1. *This can be used when the MCU wants to make sure that it is the end of the transmission in High Speed Data Transferring (HSDT) mode.*
2. *This can be used when data lanes are to be kept in High Speed Data Transferring (HSDT) Mode.*

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Table 8: Data Type (DT) from the Display Module to the MCU

From the Display Module to the MCU								
Bit5	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Hex**	**Description**	**Short/Long Packet**
0	0	0	0	1	0	02	Acknowledge with Error Report	SPa (Short Packet)
0	0	1	0	0	0	08	End of Transmission Packet (EoTP)	SPa (Short Packet)
0	1	0	0	0	1	11	Generic Short READ Response, 1 byte returned	SPa (Short Packet)
0	1	0	0	1	0	12	Generic Short READ Response, 2 byte returned	SPa (Short Packet)
0	1	1	0	1	0	1A	Generic Long READ Response	LPa (Long Packet)
0	1	1	1	0	0	1C	DCS Read Long Response	LPa (Long Packet)
1	0	0	0	0	1	21	DCS Read Short Response, 1 byte returned	SPa (Short Packet)
1	0	0	0	1	0	22	DCS Read Short Response, 2 byte returned	SPa (Short Packet)

The receiver will ignore other Data Types (DT) if they are not defined in Table 7 and Table 8.

4.1.3.1.3.2. Packet Data (PD) in a Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is placed after Data Type (DT) of the Data Identification (DI) and indicates a Short Packet (SPa) is to be sent. Packet Data (PD) of a Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1. The sending order of the Packet Data (PD) is that Data 0 is sent first and the Data 1 is sent last. Bits of Data 1 are set to 0 if the information length is 1 byte. Packet Data (PD) of a Short Packet (SPa), when the length of the information is 1 or 2 bytes and Virtual Channel (VC) is 0, are illustrated for reference purposes below.

Packet Data (PD) information:

• Data 0: 26hex (Display Command Set (DCS) with 1 Parameter => DI (Data Type (DT)) = 15hex)

• Data 1: 01hex (DCS's parameter)

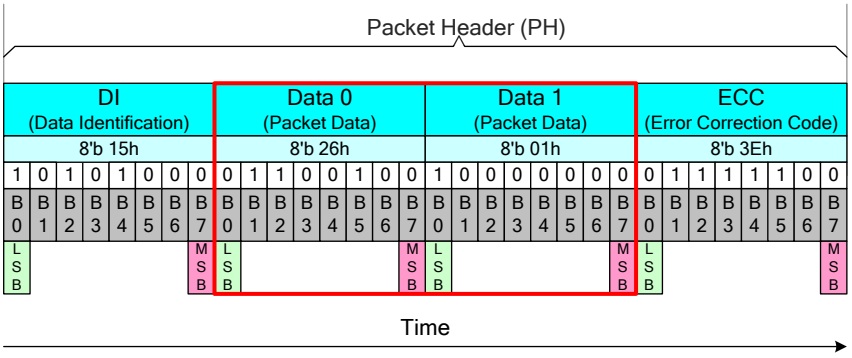


Figure 42: Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

• Data 0: 10hex (DCS without parameter => DI (Data Type (DT)) = 05hex)

• Data 1: 00hex (Null)

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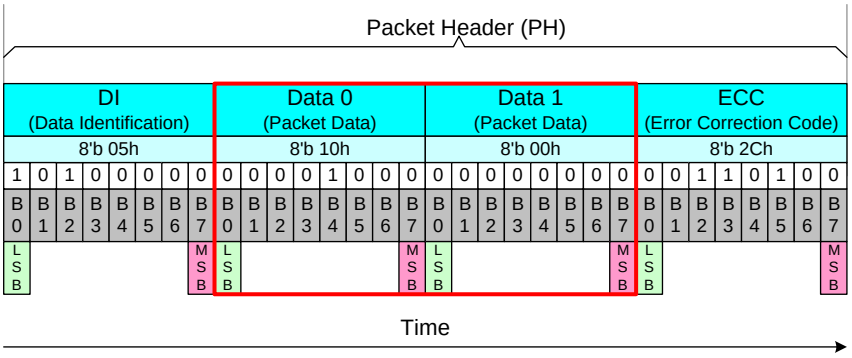


Figure 43: Packet Data (PD) for Short Packet (SPa), 1 Byte Information

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4.1.3.1.3.3. Word Count (WC) in a Long Packet (LPa)

Word Count (WC) of the Long Packet (LPa) is placed after Data Type (DT) of the Data Identification (DI) and indicates that a Long Packet (LPa) is to be sent. Word Count (WC) indicates the amount of data bytes of the Packet Data (PD) that is to be sent after the Packet Header (PH). The location of the Word Count (WC) in a Long Packet is the same as which of the Packet Data (PD) in a Short Packet (SPa), as shown in Figure 45. Word Count (WC) of the Long Packet (LPa) consists of 2 bytes. The sending order of these 2 bytes of the Word Count (WC) is that the Least Significant (LS) Byte is sent first, and the Most Significant (MS) Byte is sent last. Word Count (WC) of a Long Packet (LPa) is illustrated for reference purposes below.

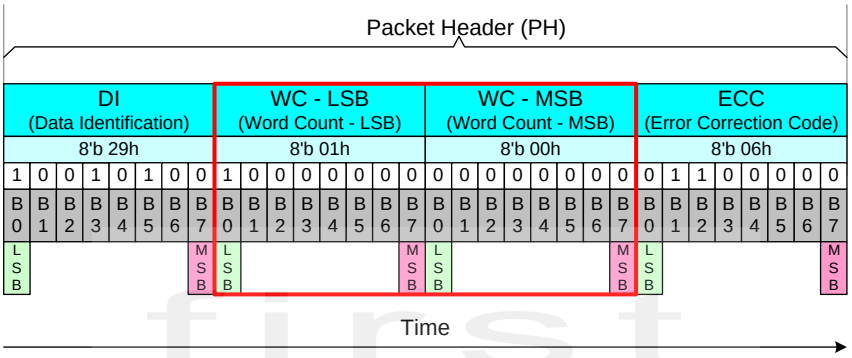


Figure 44: Word Count (WC) in a Long Packet (LPa)

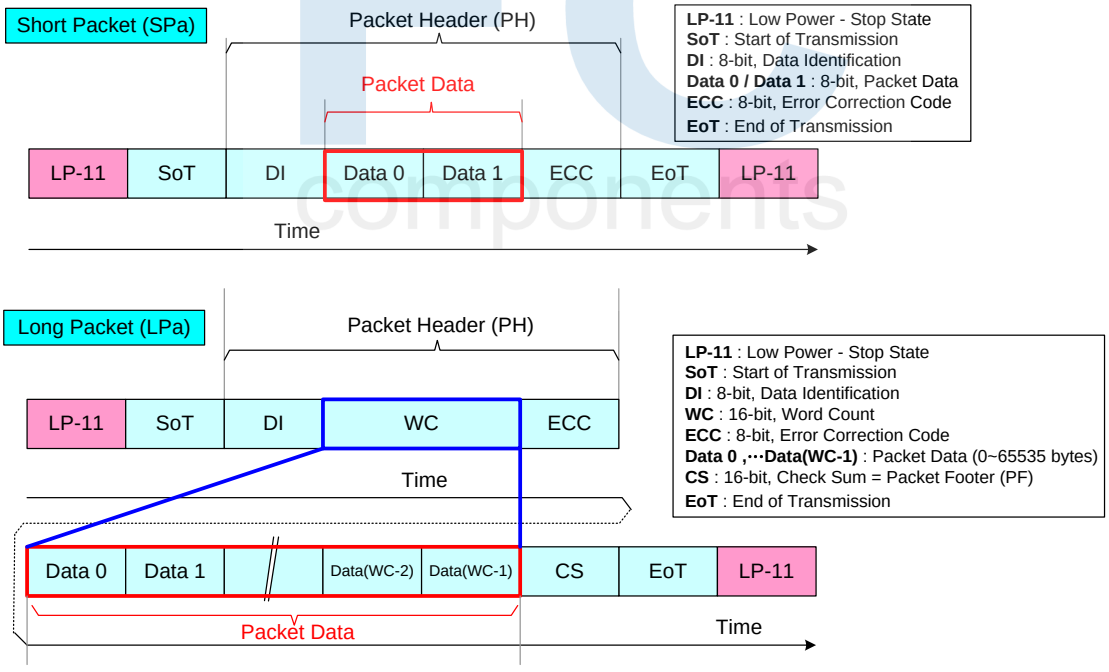


Figure 45: Packet Data in Short and Long Packets

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4.1.3.1.3.4. Error Correction Code (ECC)

The Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors. The ECC protects the following fields:

- Short Packet (SPa): Data Identification (DI) byte (8 bits: D [0…7]), Packet Data (PD) bytes (16 bits: D [8…23]) and ECC (8 bits: P [0…7])
- Long Packet (LPa): Data Identification (DI) byte (8 bits: D [0…7]), Word Count (WC) bytes (16 bits: D [8…23]) and ECC (8 bits: P [0…7])

D [23…0] and P [7…0] are illustrated for reference purposes below.

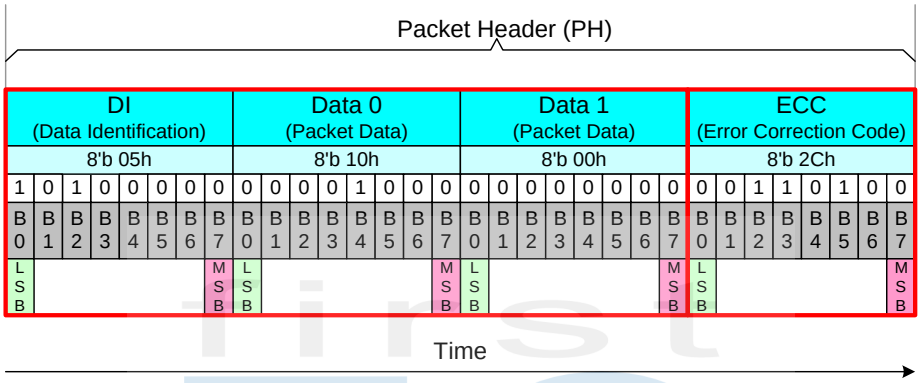


Figure 46: D [23…0] and P [7…0] in a Short Packet (SPa)

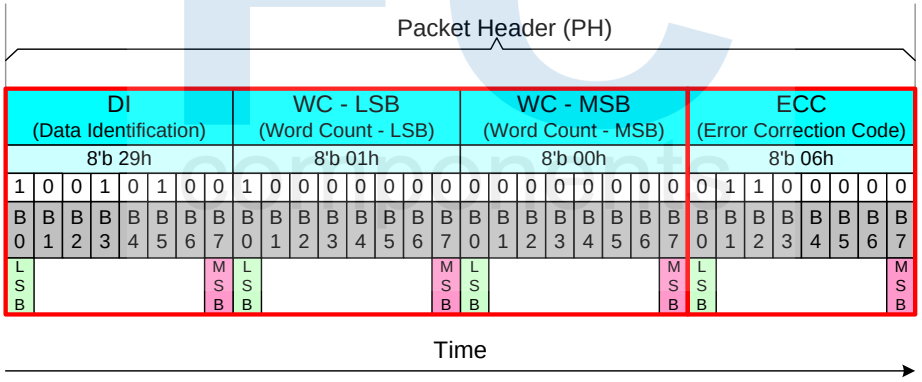


Figure 47: D [23…0] and P [7…0] in a Long Packet (LPa)

Error Correction Code (ECC) can recognize one or several error(s) and can only correct one-bit error. Bits (P [7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' presents the XOR function (Pn is 1 if there is odd number of 1, and Pn is 0 if there is even number of 1), as follows.

• P7 = 0

• P6 = 0

• P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

• P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

• P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

• P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

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• P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

• P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to 0 because Error Correction Code (ECC) is based on 64 bit value (D [63…0]), but this implementation is based on 24 bit value (D [23…0]). Therefore, only 6 bits are needed (P [5…0]) for Error Correction Code (ECC).

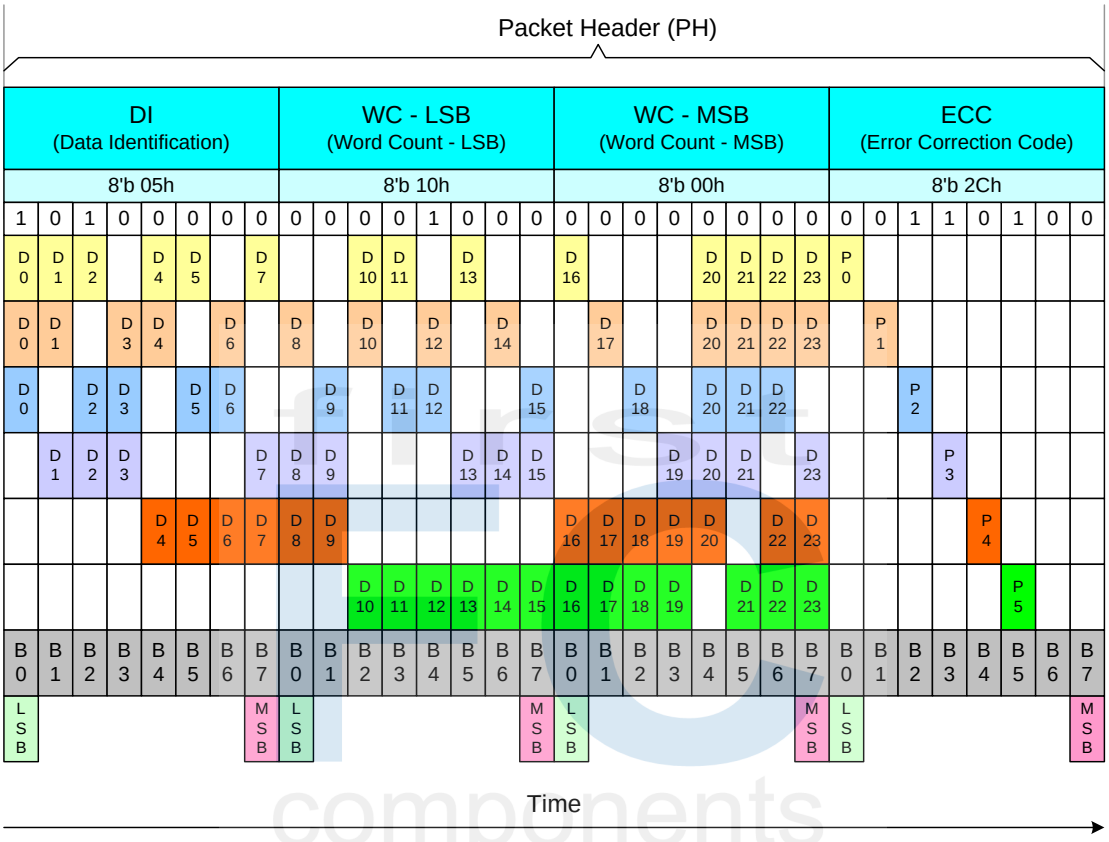


Figure 48: XOR Function on a Short Packet (SPa)

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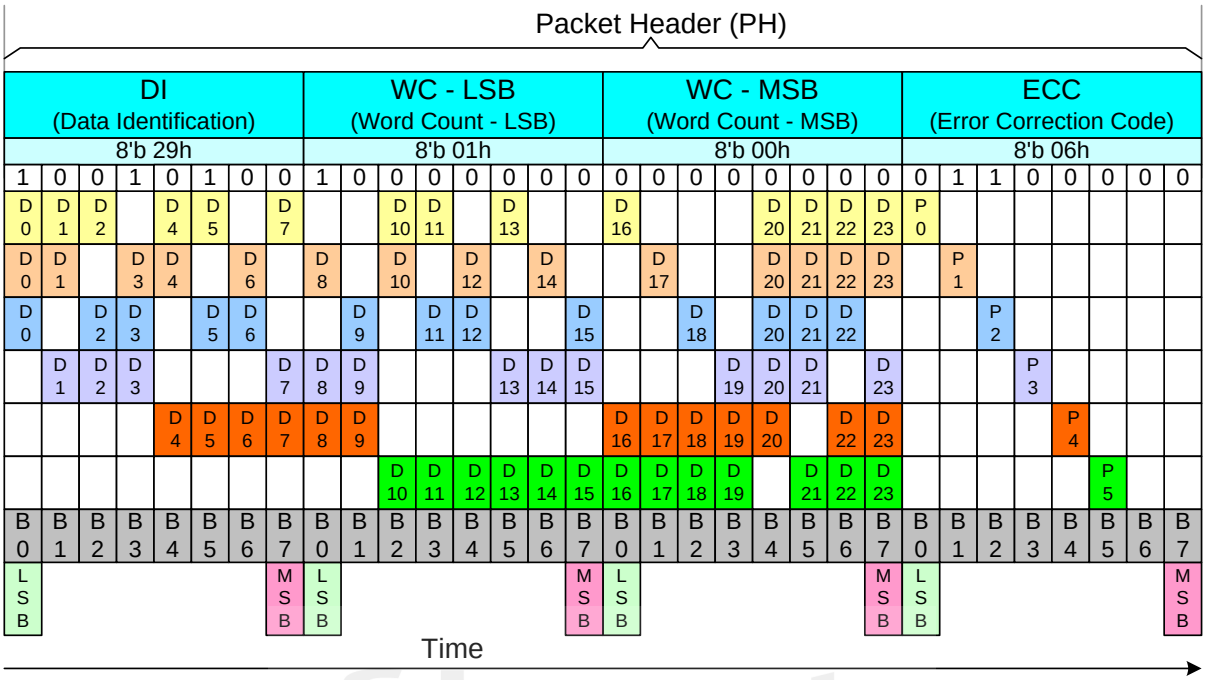


Figure 49: XOR Function on a Long Packet (LPa)

The transmitter (= the MCU or the Display Module) will send data bits D [23…0] and Error Correction Code (ECC) P [7…0]. The receiver (= the Display module or the MCU) will calculate the Internal Error Correction Code (IECC) and compare the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have performed the XOR function. The result of this function is PO [7…0]. This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for reference purposes below.

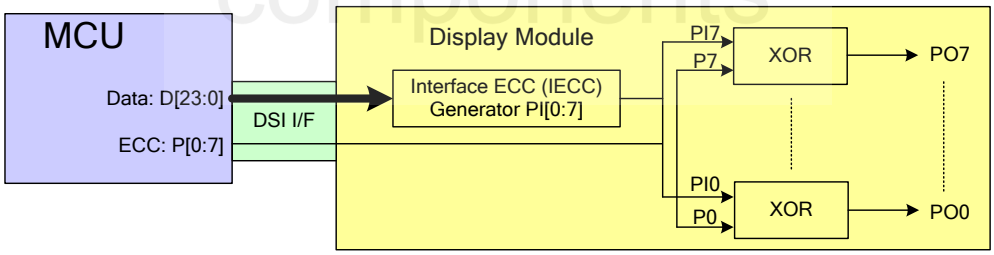


Figure 50: Internal Error Correction Code (IECC) on the Display Module (= the Receiver)

The sent data bits (D [23…0]) and ECC (P [7…0]) are correctly received if the value of the PO [7…0]) is 00h.

The sent data bits (D [23…0]) and ECC (P [7…0]) are not correctly received if the value of the PO [7…0]) is not 00h.

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ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	0	0	0	0	0	0	03h
XOR(ECC, IECC) => PO[7…0]	0	0	0	0	0	0	0	0	= 00h => No Error
	L							M	
	S							S	
	B							B	

Figure 51: Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC, IECC) => PO[7…0]	0	0	1	1	0	0	0	0	= 0Ch => Error
	L							M	
	S							S	
	B							B	

Figure 52: Internal XOR Calculation between ECC and IECC Values - Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) function is not used for data values D [23…0] on the transmitter side. The number of the errors (one or more) can be defined when the value of the PO [7…0] is compared to the values in the following table.

Table 9: One Bit Error Value of the Error Correction Code (ECC)

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D [0]	0	0	0	0	0	1	1	1	07h
D [1]	0	0	0	0	1	0	1	1	0Bh
D [2]	0	0	0	0	1	1	0	1	0Dh
D [3]	0	0	0	0	1	1	1	0	0Eh
D [4]	0	0	0	1	0	0	1	1	13h
D [5]	0	0	0	1	0	1	0	1	15h
D [6]	0	0	0	1	0	1	1	0	16h
D [7]	0	0	0	1	1	0	0	1	19h
D [8]	0	0	0	1	1	0	1	0	1Ah
D [9]	0	0	0	1	1	1	0	0	1Ch
D [10]	0	0	1	0	0	0	1	1	23h
D [11]	0	0	1	0	0	1	0	1	25h
D [12]	0	0	1	0	0	1	1	0	26h
D [13]	0	0	1	0	1	0	0	1	29h
D [14]	0	0	1	0	1	0	1	0	2Ah
D [15]	0	0	1	0	1	1	0	0	2Ch
D [16]	0	0	1	1	0	0	0	1	31h
D [17]	0	0	1	1	0	0	1	0	32h
D [18]	0	0	1	1	0	1	0	0	34h
D [19]	0	0	1	1	1	0	0	0	38h
D [20]	0	0	0	1	1	1	1	1	1Fh
D [21]	0	0	1	0	1	1	1	1	2Fh
D [22]	0	0	1	1	0	1	1	1	37h
D [23]	0	0	1	1	1	0	1	1	3Bh

An error is detected if the value of the PO [7…0] is in Table 9, and the receiver can correct this one bit error

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because this found value also defines the location of the corrupt bit, e.g.

- PO [7…0] = 0Eh
- The bit of the data (D [23…0]), that is not correct, is D [3]

More than one error is detected if the value of the PO [7…0] is not in Table 9,for example, PO [7…0] = 0Ch.

4.1.3.1.4. Packet Data (PD) in a Long Packet (LPa)

Packet Data (PD) of a Long Packet (LPa) is placed after the Packet Header (PH) of a Long Packet (LPa). The amount of the data bytes is defined in the section “4.1.3.1.3.3 Word Count (WC) in a Long Packet (LPa)”.

4.1.3.1.5. Packet Footer (PF) in a Long Packet (LPa)

Packet Footer (PF) of a Long Packet (LPa) is placed after the Packet Data (PD) of a Long Packet (LPa). The Packet Footer (PF) is a checksum value that is calculated from the Packet Data of the Long Packet (LPa). The checksum uses a 16-bit Cyclic Redundancy Check (CRC) value which is generated by a polynomial X16+X12+X5+X0, as illustrated below.

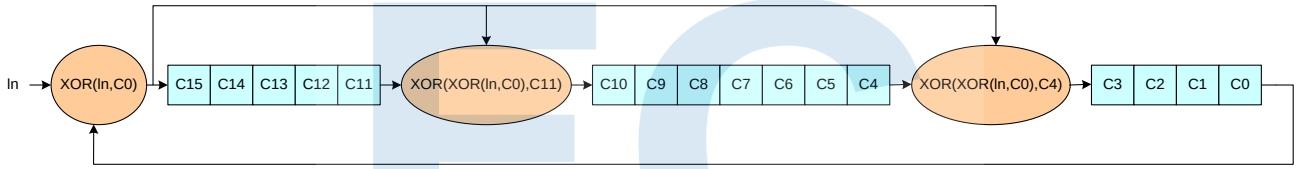
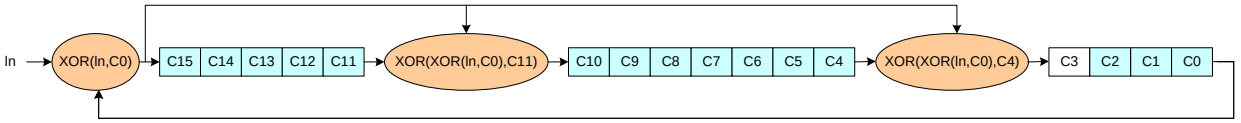


Figure 53: 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit which is inputted into the 16-bit Cyclic Redundancy Check (CRC). An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of a Long Packet (LPa) is 01h, is illustrated (step-by-step) below.



Step	In	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11(Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4(Step-1))	C3	C2	C1	C0	C0
0	X	X	1	1	1	1	1	X	1	1	1	1	1	1	1	X	1	1	1	1	X
1	1(LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
8	0(MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
	1 byte	CRC result	0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0	
			MSB																	LSB	

Figure 54: CRC Calculation – Packet Data (PD) is 01h

The value of the Packet Footer (PF) is 1E0Eh in this example (Command 01h has been sent), and is illustrated

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below.

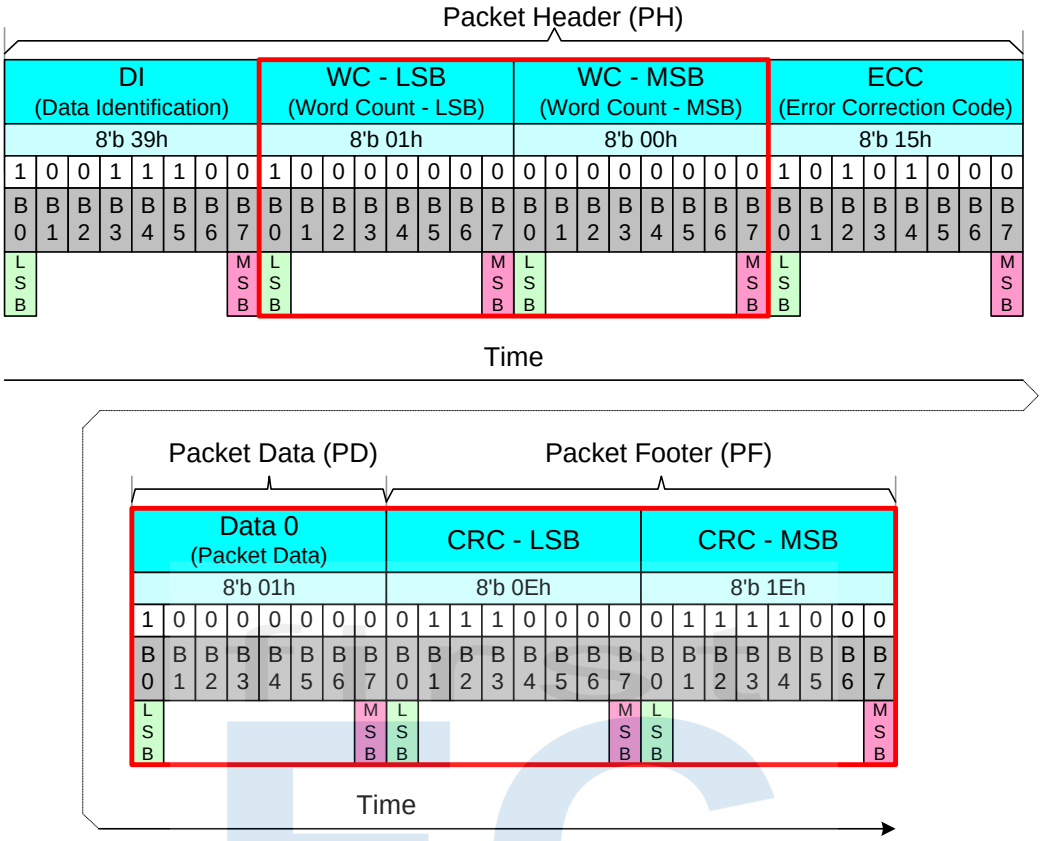


Figure 55: Packet Footer (PF) Example

The receiver calculates its checksum value from the received Packet Data (PD). The receiver compares its checksum and the Packet Footer (PF) that the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the checksum of the receiver and Packet Footer (PF) are equal. The received Packet Data (PD) and Packet Footer (PF) are not correct if the checksum of the receiver and Packet Footer (PF) are not equal.

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4.1.3.2. Packet Transmissions

4.1.3.2.1. Packet from the MCU to the Display Module

4.1.3.2.1.1. Display Command Set (DCS)

Display Command Set (DCS), defined in the section “5.3Page 0 Command Description”, is used from the MCU to the display module. This Display Command Set (DCS) is always defined in the Data 0 of the Packet Data (PD), and is included in Short Packet (SPa) and Long packet (LPa), as illustrated below.

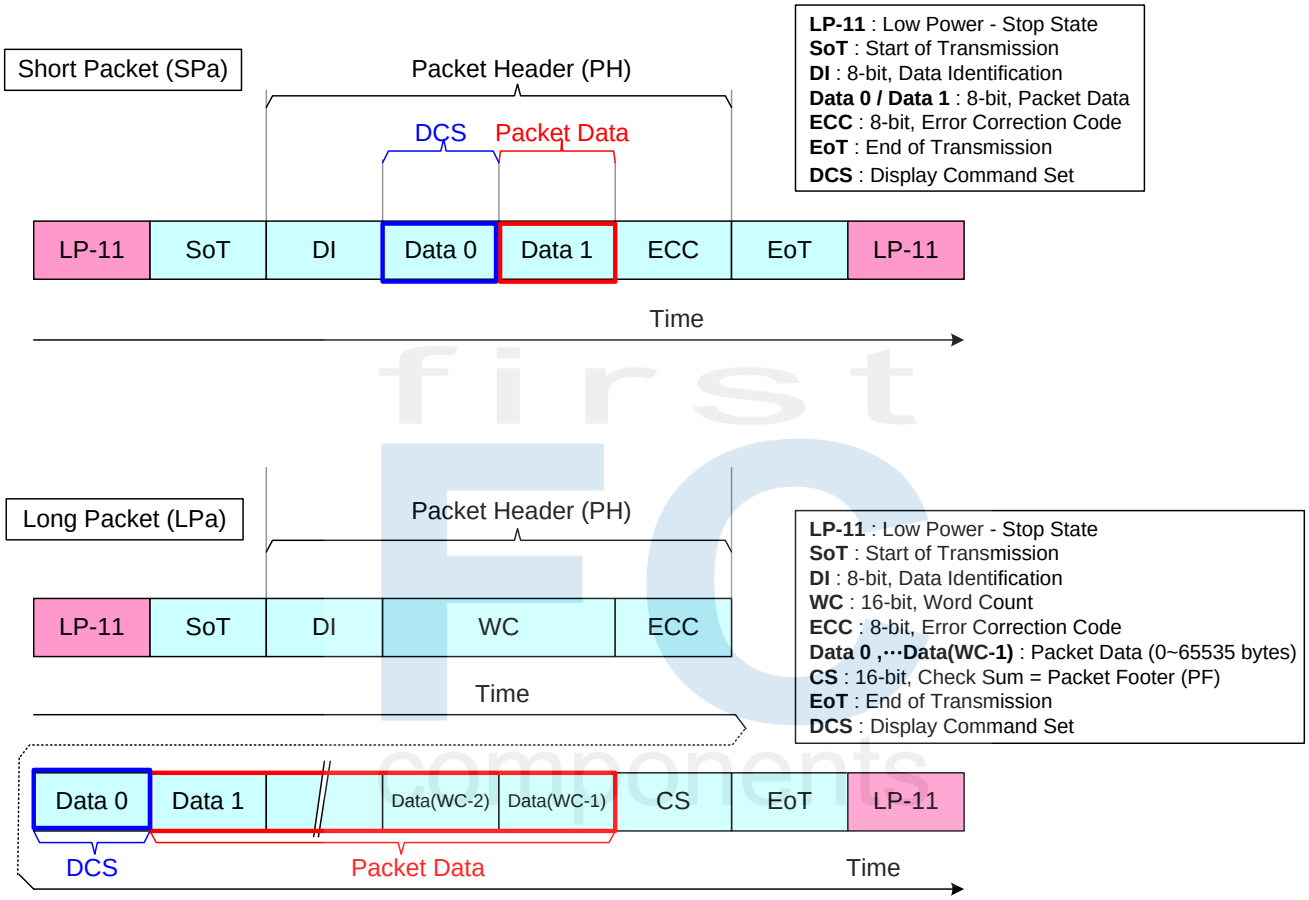


Figure 56: Display Command Set (DCS) in Short Packet (SPa) and Long Packet (LPa)

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4.1.3.2.1.2. Display Command Set (DCS) Write, No Parameter (DCSWN-S)

"Display Command Set (DCS) Write, No Parameter", which is defined in Data Type (DT, 00 0101b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in a table below.

Table 10: Display Command Set (DCS) Write, No Parameters (DCSWN-S)

Command
NOP (00h)
Software Reset (01h)
Sleep In(10h)
Sleep Out (11h)
Normal Display Mode On (13h)
All Pixel Off (22h)
All Pixel On (23h)
Display Off (28h)
Display ON (29h)
Tearing Effect Line OFF (34h)
Idle Mode Off (38h)
Idle Mode On (39h)
Stop Transition (59h)

A Short Packet (SPa) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 00 0101b
- Packet Data (PD)
  - ✧ Data 0: "Sleep In (10h)", Display Command Set (DCS)
  - ✧ Data 1: Always 00hex
- Error Correction Code (ECC)

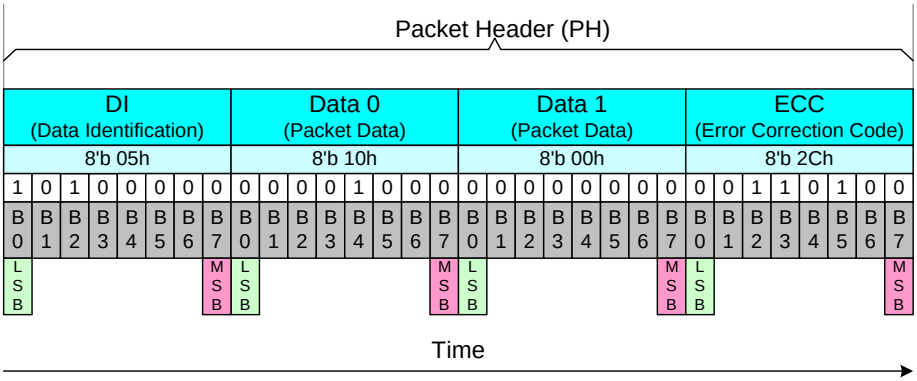


Figure 57: Display Command Set (DCS) Write, No Parameter (DCSWN-S) - Example

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4.1.3.2.1.3. Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

"Display Command Set (DCS) Write, 1 Parameter" (DCSW1-S), which is defined in Data Type (DT, 01 0101b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in the table below.

Table 11: Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

Command
Gamma Curve Set (26h)
Memory Write (2Ch), Note
Tearing Effect Line ON(35h)
Memory Access Control (36h)
Interface Pixel Format (3Ah)
Memory Write Continue (3Ch), Note
Write Display Brightness (51h)
Write CTRL Display (53h)
Write Power Save (55h)
Write Idle Mode Color (80h)

Note: One Subpixel has been written

A Short Packet (SPa) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 01 0101b
- Packet Data (PD)
  - ✧ Data 0: "Gamma Set (26h)", Display Command Set (DCS)
  - ✧ Data 1: 01hex, Parameter of the DCS
- Error Correction Code (ECC)

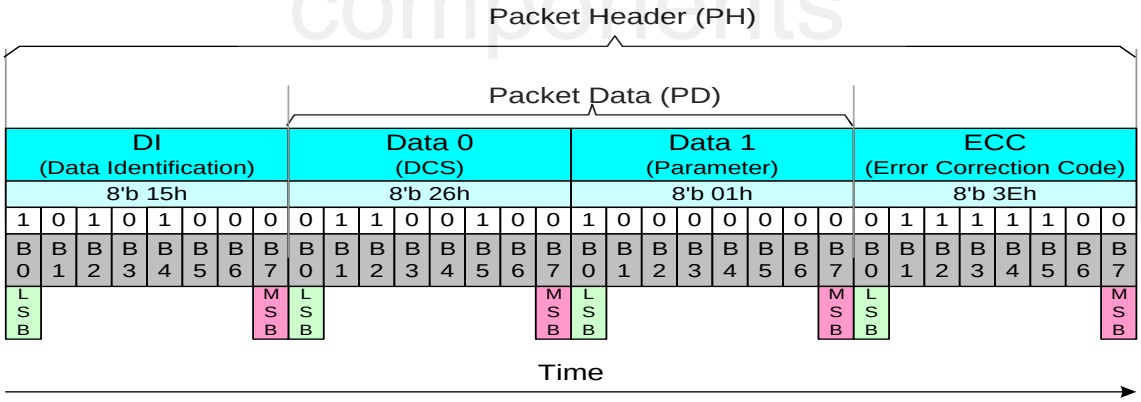


Figure 58: Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) – Example

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4.1.3.2.1.4. Display Command Set (DCS) Write Long (DCSW-L)

"Display Command Set (DCS) Write Long" (DCSW-L), which is defined in Data Type (DT, 11 1001b), is always used in a Long Packet (LPa) from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters) are defined in a table below.

Table 12: Display Command Set (DCS) Write Long (DCSW-L)

Command
NOP (00h), Note 1
Software Reset (01h), Note 1
Sleep In(10h), Note 1
Sleep Out (11h), Note 1
Normal Display Mode On (13h), Note 1
All Pixel Off (22h) , Note 1
All Pixel On (23h) , Note 1
Gamma Curve Set (26h), Note 2
Display Off (28h), Note 1
Display ON (29h), Note 1
Memory Write (2Ch), Note 2
Tearing Effect Line OFF (34h), Note 1
Tearing Effect Line ON (35h), Note 2
Memory Access Control (36h), Note 2
Idle Mode Off (38h) , Note 1
Idle Mode On (39h) , Note 1
Interface Pixel Format (3Ah), Note 2
Memory Write Continue (3Ch), Note 2
Set Tear Scan Line(44h)
Write Display Brightness (51h), Note 2
Write CTRL Display (53h), Note 2
Write Power Save(55h), Note 2
Stop Transition (59h), Note 1
Write CABC Minimum Brightness (5Eh) , Note 2
Set Transition Time(68h)
Write Idle Mode Color (80h), Note 2

Notes:

1. Short Packet (SPa) can also be used; See the section "4.1.3.2.1.2 Display Command Set (DCS) Write, No Parameter (DCSWN-S)".

2. Short Packet (SPa) can also be used; See the section "4.1.3.2.1.3 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)".

A Long Packet (LPa) with one command (No Parameter) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - ✧ Word Count (WC): 0001h
- Error Correction Code (ECC)

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- Packet Data (PD): Data 0: “Sleep In (10h)”, Display Command Set (DCS)
- Packet Footer (PF)

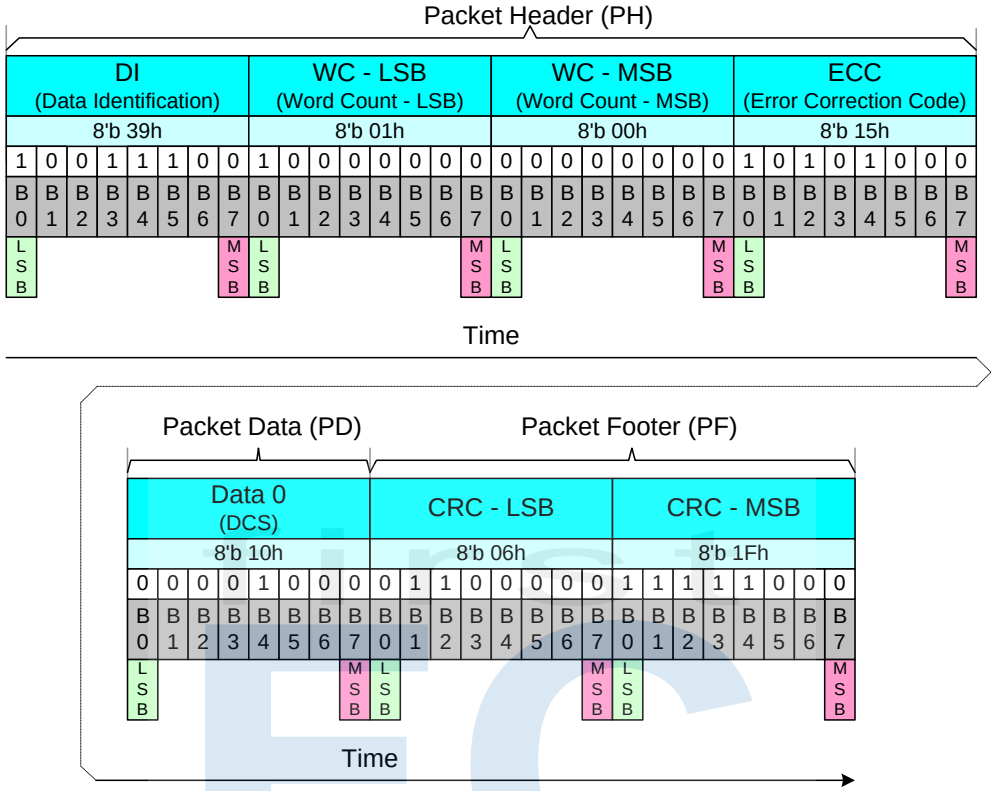


Figure 59: Display Command Set (DCS) Write Long (DCSW-L) with DCS Only - Example

A Long Packet (LPa) with one Write (1 parameter) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - ✧ Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
  - ✧ Data 0: “Gamma Set (26h)”, Display Command Set (DCS)
  - ✧ Data 1: 01hex, Parameter of the DCS
- Packet Footer (PF)

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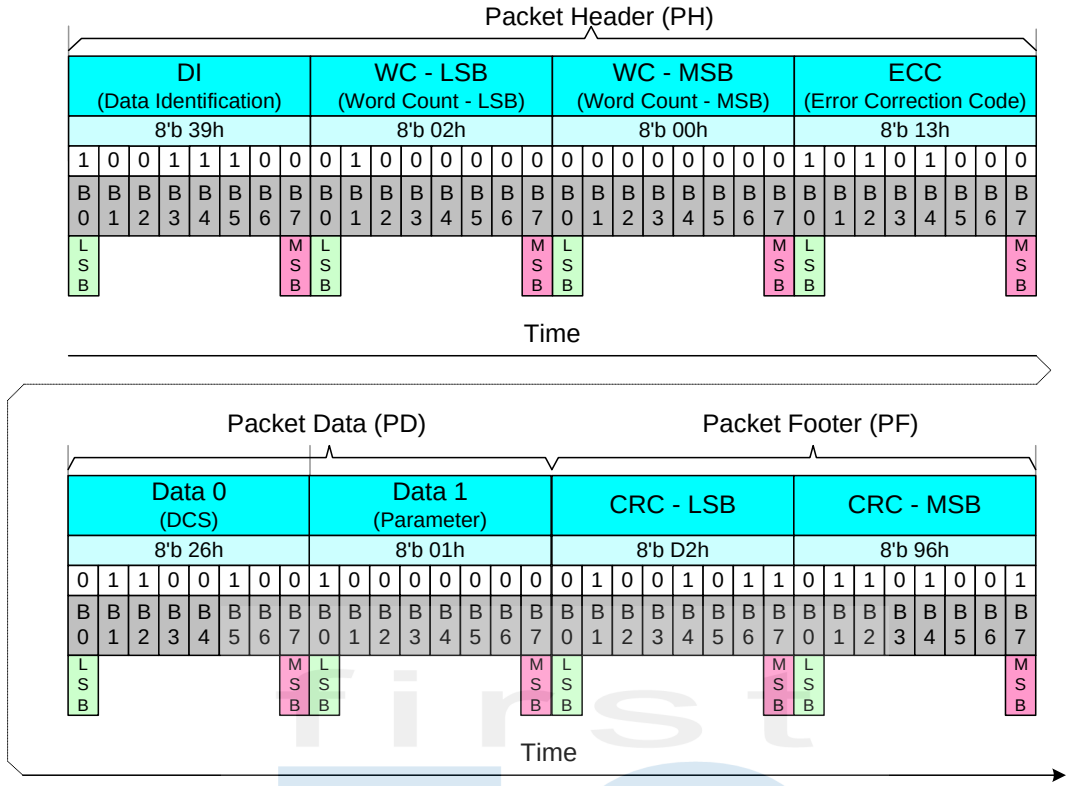


Figure 60: Display Command Set (DCS) Write Long with DCS and 1 Parameter - Example

A Long Packet (LPa) with one Write (4 parameters) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - ✧ Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
  - ✧ Data 0: “Column Address Set (2Ah)” (For example only), Display Command Set (DCS)
  - ✧ Data 1: 00hex, 1st Parameter of the DCS, Start Column SC [15…8]
  - ✧ Data 2: 12hex, 2nd Parameter of the DCS, Start Column SC [7…0]
  - ✧ Data 3: 01hex, 3rd Parameter of the DCS, End Column EC [15…8]
  - ✧ Data 4: EFhex, 4th Parameter of the DCS, End Column EC [7…0]
- Packet Footer (PF)

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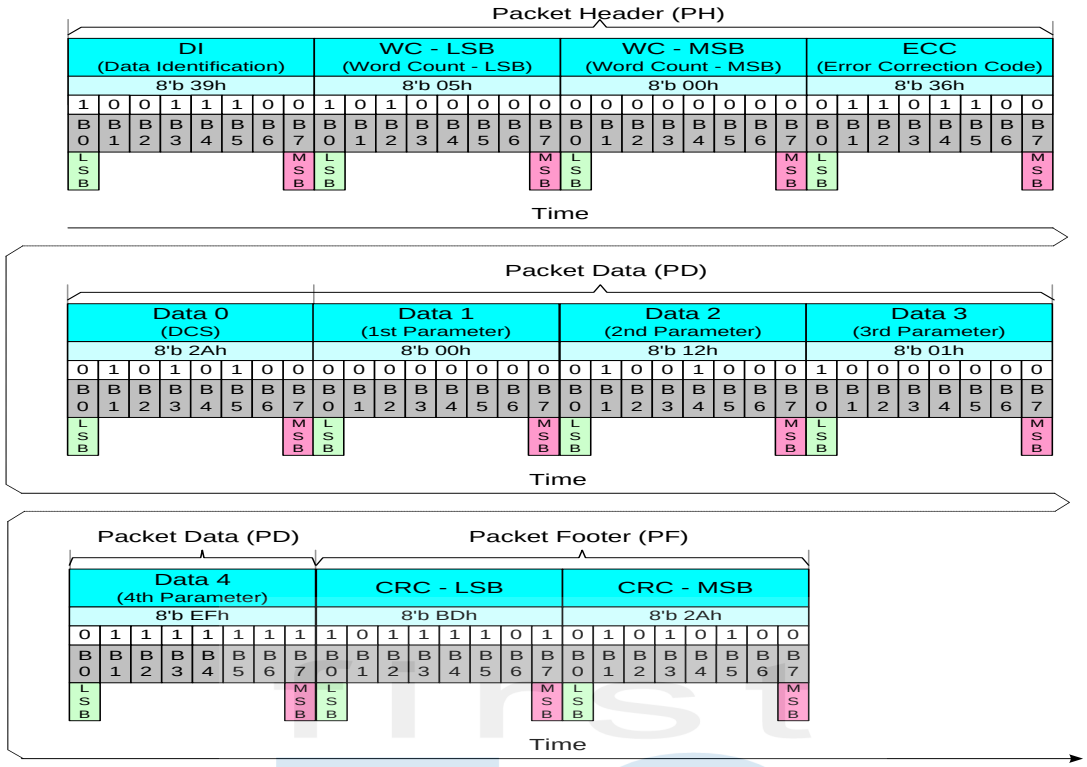


Figure 61: Display Command Set (DCS) Write Long with DCS and 4 Parameters - Example

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4.1.3.2.1.5. Display Command Set (DCS) Read, No Parameter (DCSRN-S)

"Display Command Set (DCS) Read, No Parameter" (DCSRN-S), which is defined in Data Type (DT, 00 0110b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in the table below.

Table 13: Display Command Set (DCS) Read, No Parameter (DCSRN-S)

Command
Read Number of the Errors on DSI (05h)
Read Display Power Mode (0Ah)
Read Display MADCTL (0Bh)
Read Display Pixel Format (0Ch)
Read Display Image Mode (0Dh)
Read Display Signal Mode (0Eh)
Read Display Self-Diagnostic Result (0Fh)
Get Tear Scan Line(45h)
Read Display Brightness Value (52h)
Read CTRL Value Display (54h)
Read Power Save (56h)
Read CABC Minimum Brightness (5Fh)
Get Transition Time(69h)
Read Idle Mode Color(81h)
Read DDB Start (A1h)
Read DDB Continue (A8h)
Read First Checksum(AAh)
Read Continue Checksum (AFh)
Read ID1 (DAh)
Read ID2 (DBh)
Read ID3 (DCh)

The MCU has to define to the display module the maximum size of the returned packet. The command, which is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and is used in a Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to the display module. This sequence is illustrated for reference purposes below.

Step 1:

The MCU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module.

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 11 0111b
- Maximum Return Packet Size (MRPS)
  - ✧ Data 0: 01hex
  - ✧ Data 1: 00hex
- Error Correction Code (ECC)

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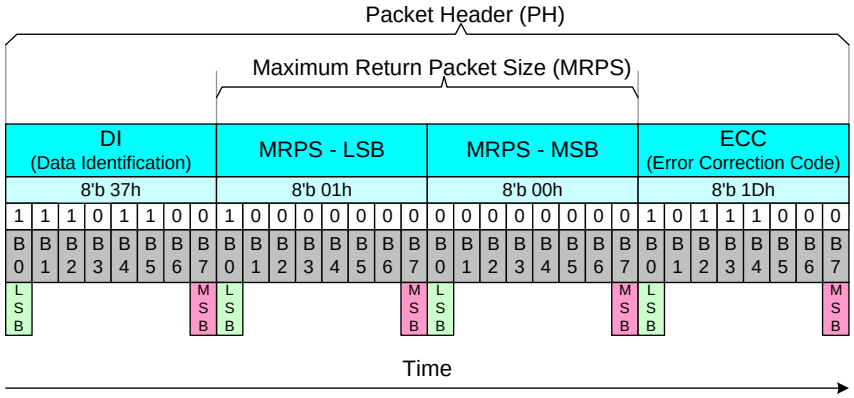


Figure 62: Set Maximum Return Packet Size (SMRPS-S) - Example

Step 2:

The MCU wants to receive the value of the "Read ID1 (DAh)" from the display module when the MCU sends "Display Command Set (DCS) Read, No Parameter" to the display module.

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 00 0110b
- Packet Data (PD)
  - ✧ Data 0: "Read ID1 (DAh)", Display Command Set (DCS)
  - ✧ Data 1: Always 00hex
- Error Correction Code (ECC)

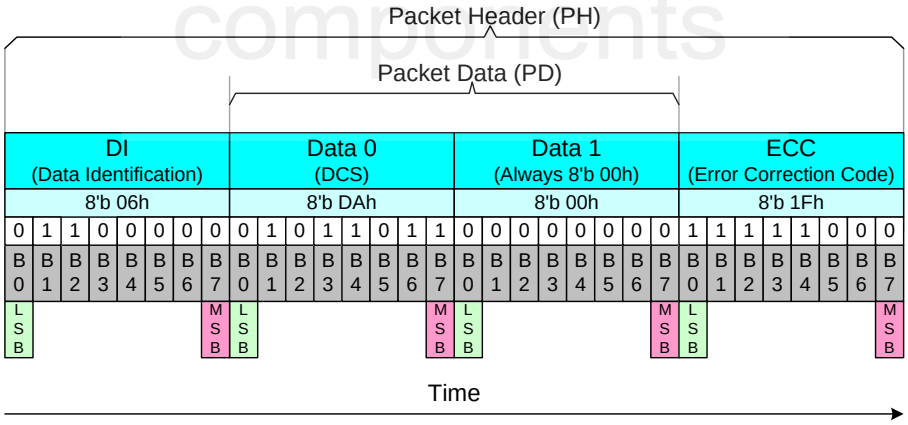


Figure 63: Display Command Set (DCS) Read, No Parameter (DCSRN-S) - Example

Step 3:

The display module can send 2 different information to the MCU after Bus Turnaround (BTA):

1. An acknowledge with Error Report (AwER), which is used in a Short Packet (SPa), if there is an error when receiving a command. See the section "4.1.3.2.2.2 Acknowledge with Error Report (AwER)".

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2. Information of the received command, which can be a Short Packet (SPa) or a Long Packet (LPa).

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4.1.3.2.1.6. Null Packet, No Data (NP-L)

"Null Packet, No Data" (NP-L), which is defined in Data Type (DT, 001001b), is always used in a Long Packet (LPa) from the MCU to the display module. The purpose of this command is to keep data lanes in the high speed mode (HSDT) if necessary. The display module can ignore the Packet Data (PD) that the MCU sends.

A Long Packet (LPa) with 5 random data bytes of the Packet Data (PD) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 00 1001b
- Word Count (WC)
  - ✧ Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
  - ✧ Data 0: 89hex (Random data)
  - ✧ Data 1: 23hex (Random data)
  - ✧ Data 2: 12hex (Random data)
  - ✧ Data 3: A2hex (Random data)
  - ✧ Data 4: E2hex (Random data)
- Packet Footer (PF)

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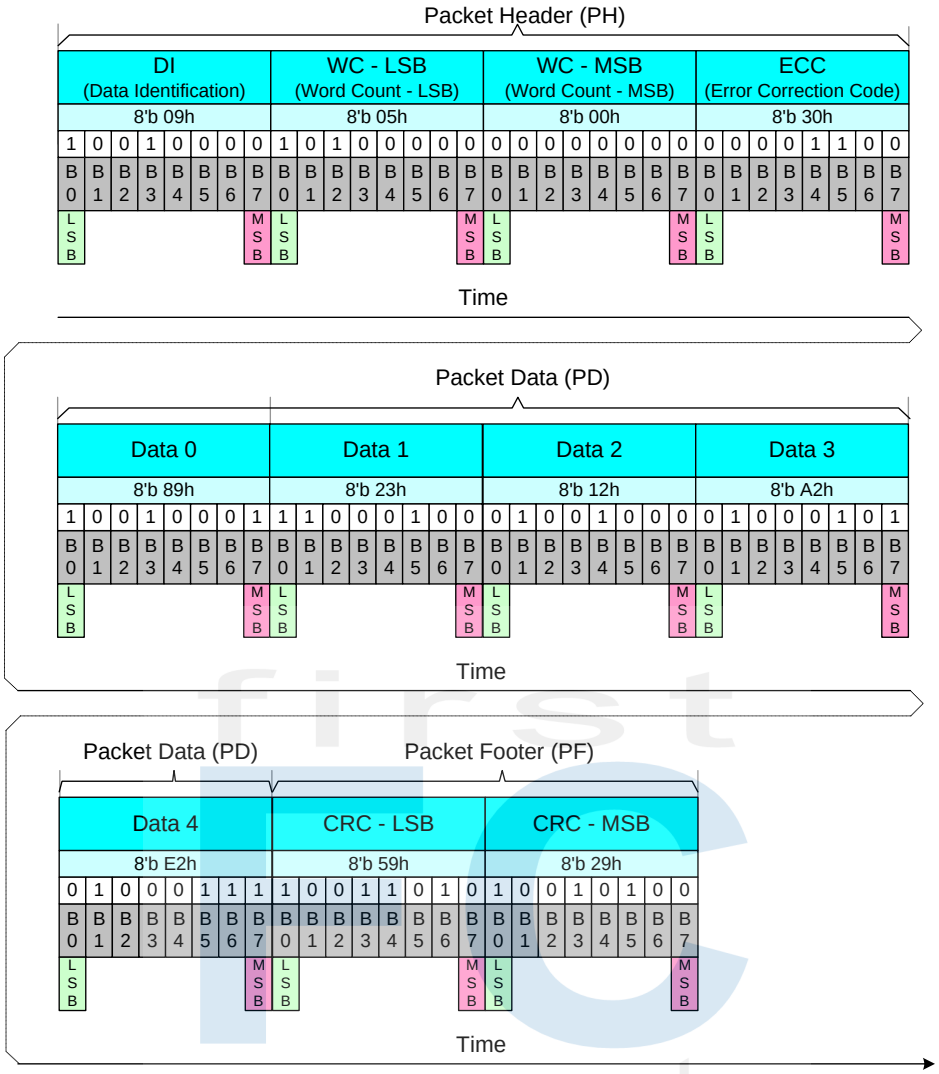


Figure 64: Null Packet, No Data (NP-L) - Example

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4.1.3.2.1.7. End of Transmission Packet (EoTP)

"End of Transmission Packet" (EoTP), which is an interface level function and defined in Data Type (DT, 00 1000b), is always used in a Short Packet (SPa) from the MCU to the display module. The purpose of this command is to terminate the high Speed Data Transmission (HSDT) mode properly when EoTP is added after the last payload packet before "End of Transmission" (EoT).

The MCU can decide if it wants to use the "End of Transmission Packet" (EoTP) or not. The display shall have the capability to support both. That is, if the MCU applies the EoTP, it shall report the "DSI Protocol Violation Error" when the EoTP is not detected in the High-Speed (HS). The display module error reporting shall be enabled/disabled statistically, according to the module application.

The display module does or does not receive "End of Transmission Packet" (EoTP) from the MCU during the Low Power Data Transmission (LPDT) mode before "Mark-1" (= leaving the Escape mode) which ends the Low Power Data Transmission (LPDT) mode. The display module is not allowed to send "End of Transmission Packet" (EoTP) to the MCU during the Low Power Data Transmission (LPDT) mode. The summary of the receiving and transmitting EoTP is listed below.

Table 14: Receiving and Transmitting EoTP during LPDT

Direction	Display Module (DM) in High Speed Data Transmission (HSDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MCU => Display Module	Support With and Without EoTP	Support With and Without EoTP
Display Module => MCU	HS Mode is not available (EoTP is not available)	EoTP cannot be sent by the Display Module (DM)

A Short Packet (SPa) using a fixed format is as follows:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 00 1000b
- Packet Data (PD)
  - ✧ Data 0: 0Fhex
  - ✧ Data 1: 0Fhex
- Error Correction Code (ECC)
  - ✧ ECC: 01hex

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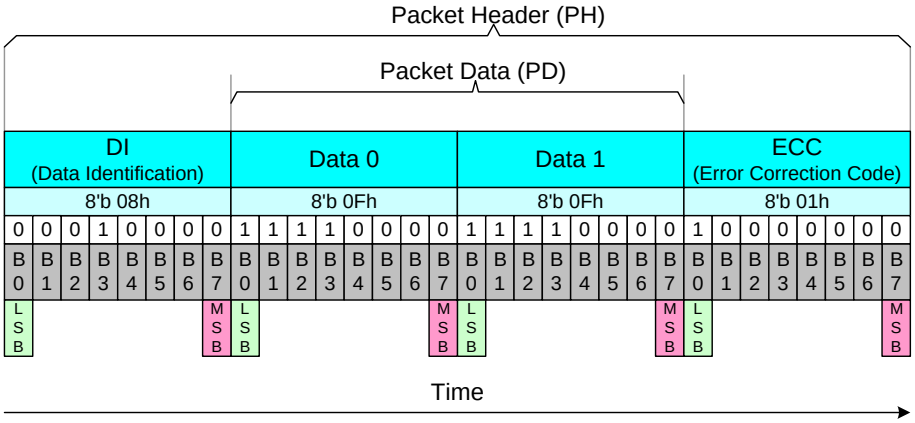


Figure 65: End of Transmission Packet (EoTP)

Some examples of the “End of Transmission Packet” (EoTP) are illustrated for reference purposes below.

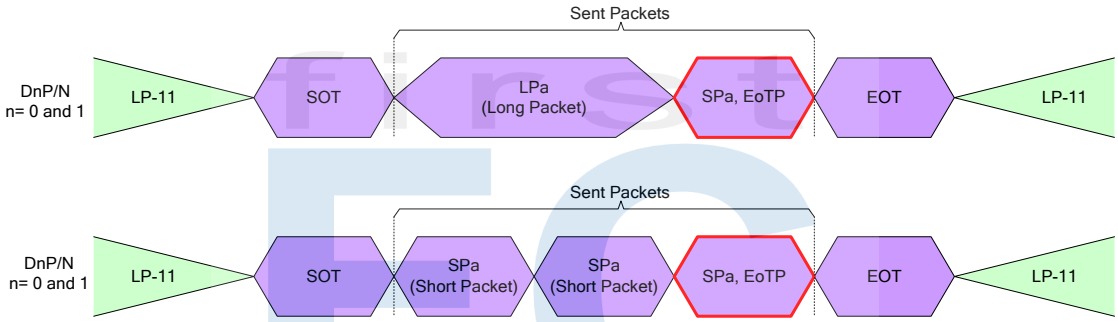


Figure 66: End of Transmission Packet (EoTP)-Examples

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4.1.3.2.2. Packet from the Display Module to the MCU

4.1.3.2.2.1. Used Packet types

The display module always uses Short Packets (SPa) or Longs Packet (LPa) when returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) (See the section “4.1.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)”) or an Acknowledge with Error Report (See the section “4.1.3.2.2.2 Acknowledge with Error Report (AwER)”).

The used packet type is defined on Data Type (DT). See the section “4.1.3.1.3.1.2 Data Type (DT)”. If the maximum size of the Packet Data (PD) could be sent in one packet, the display module should not send returned bytes in several packets. Both cases are illustrated for reference purposes below.

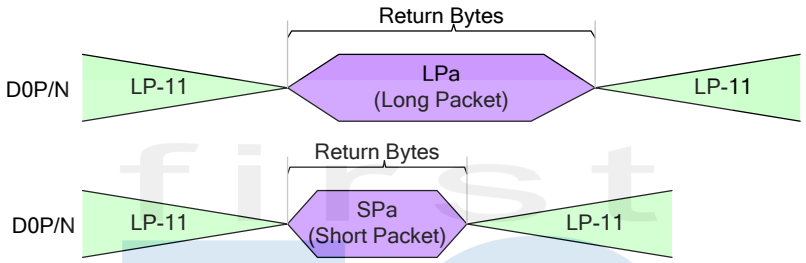


Figure 67: Return Bytes in Single Packet

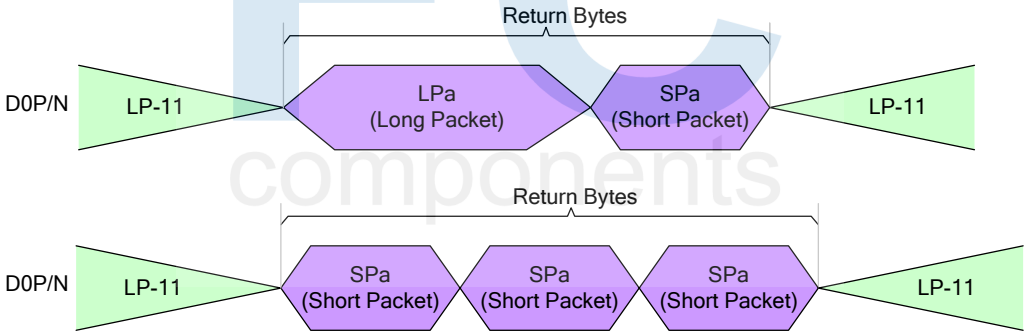


Figure 68: Return Bytes in Several Packets – Not Allowed

EXCEPTION:

The display module will return 2 packets (1st packet: Data, 2nd Packet: Acknowledge with Error Report) to the MCU when the display module receives a read command (See section “4.1.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)”), which is detected and corrected a single bit error by the EEC (See bit 8 in Table 15). These returned packets are illustrated for reference purposes below.

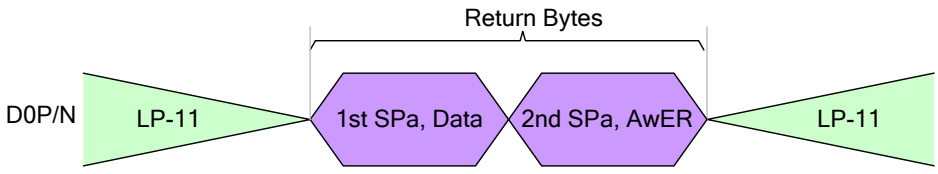


Figure 69: Exception when Returned Bytes in Several Packets

AwER = Acknowledge with Error Report

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4.1.3.2.2.2. Acknowledge with Error Report (AwER)

"Acknowledge with Error Report" (AwER), which is defined in Data Type (DT, 00 0010b), is always used in a Short Packet (SPa) from the display module to the MCU. The Packet Data (PD) can include bits, which define the current error, when the corresponding bit is set to 1, as defined in the following table.

Table 15: Error Report (AwER) Bit Definitions

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long Packet only)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to 0 internally
15	DSI Protocol Violation

These errors are included in all packages that have been received from the MCU to the display module before the Bus Turnaround (BTA). The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of a Short Packet (SPa) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 00 0010b
- Packet Data (PD)
  - ✧ Bit 8: ECC Error, single-bit (detected and corrected)
  - ✧ AwER: 0100h
- Error Correction Code (ECC)

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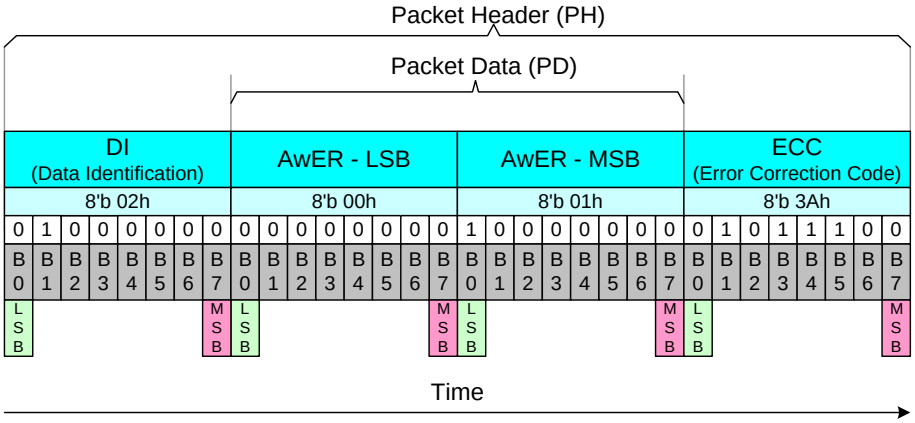


Figure 70: Acknowledge with Error Report (AwER) – Example

It is possible that the display module receives several packets, which include errors, from the MCU before the MCU performs the Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.

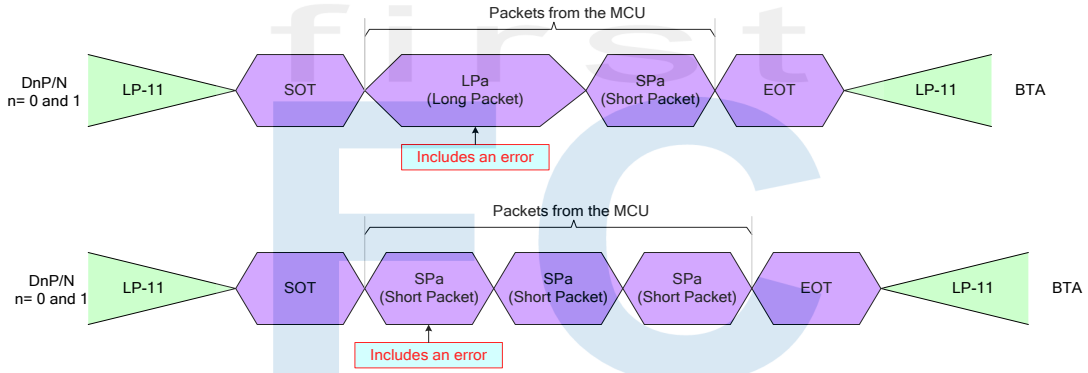


Figure 71: Errors Packets

Therefore, a method is needed to check if there are errors in the previous packets. These errors of the previous packets can be detected by “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)” commands. The bit D0 of the “Read Display Signal Mode (0Eh)” command will be set to 1 if a received packet includes an error.

The amount of packets, which include an ***ECC*** *or* ***CRC*** error, is calculated in the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h and set the bit D0 of the “Read Display Signal Mode (0Eh)” command to 0 after the MCU has read the RDNUMED register from the display module. The functionality of the RDNUMED register is illustrated for reference purposes below.

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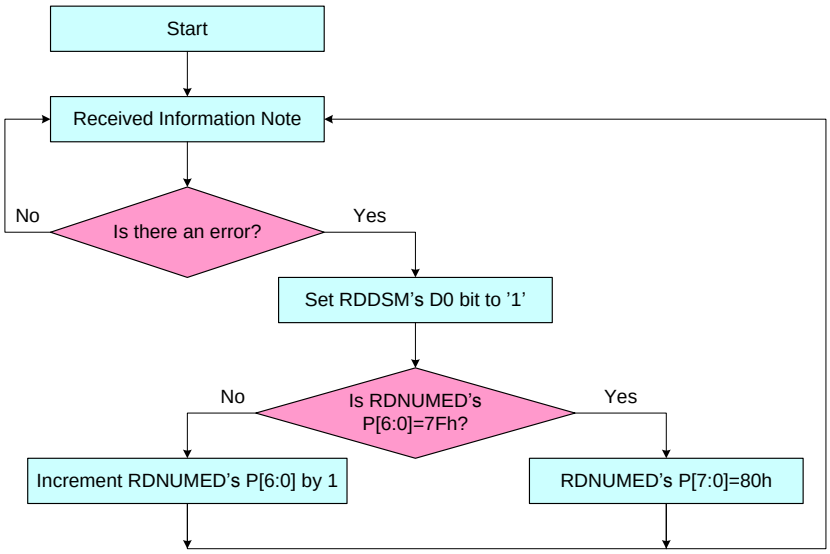


Figure 72: Flow Chart for Errors on DSI

Notes:

1. *This information can be Interface or Packet Level Communication, but it is always from the MCU to the display module.*
2. *CRC or ECC error*

4.1.3.2.2.3. DCS Read Long Response (DCSRR-L)

"DCS Read Long Response" (DCSRR-L), which is defined in Data Type (DT, 011100b), is always used in a Long Packet (LPa) from the display module to the MCU. "DCS Read Long Response" (DCSRR-L) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 01 1100b
- Word Count (WC)
  - ✧ Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
  - ✧ Data 0: 89hex
  - ✧ Data 1: 23hex
  - ✧ Data 2: 12hex
  - ✧ Data 3: A2hex
  - ✧ Data 4: E2hex
- Packet Footer (PF)

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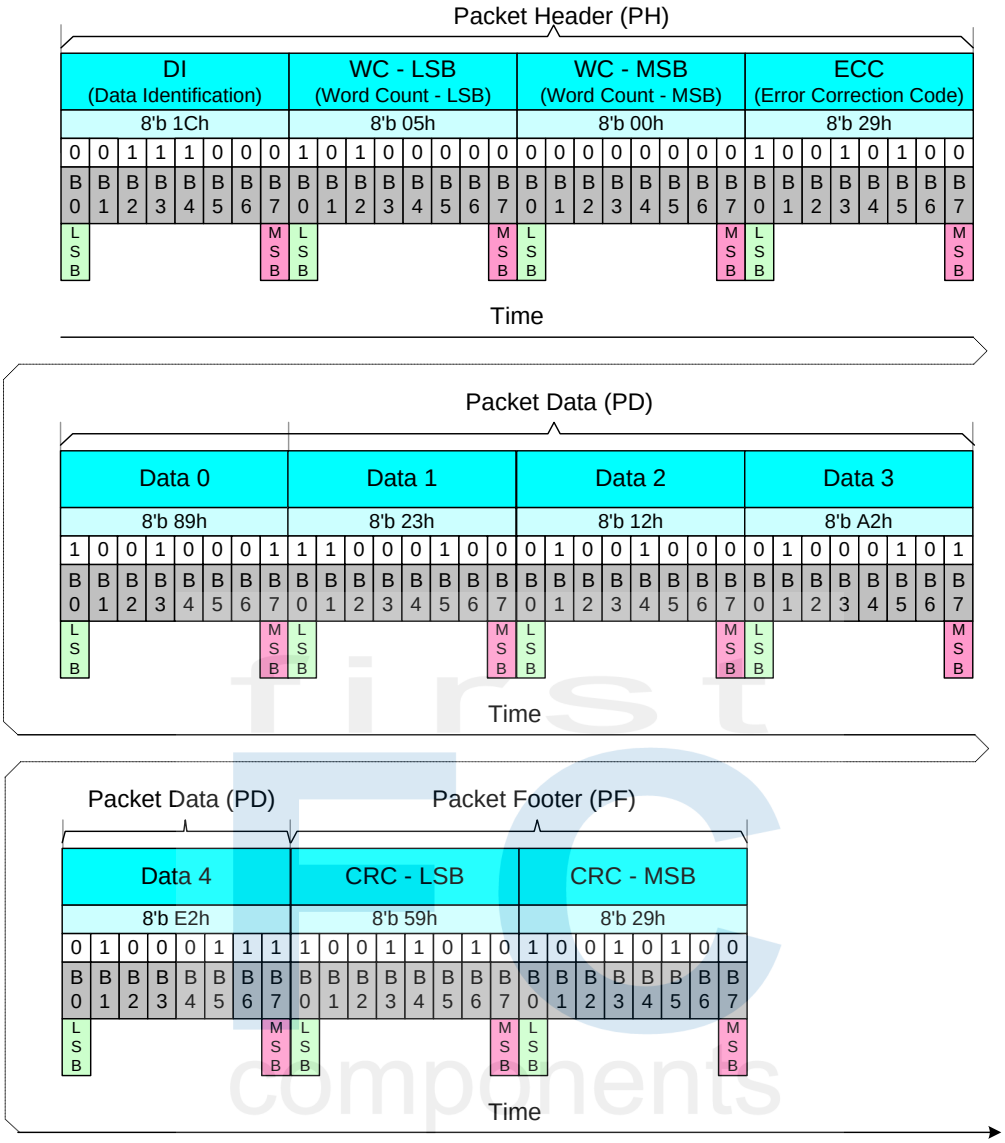


Figure 73: DCS Read Long Response (DCSRR-L) - Example

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4.1.3.2.2.4. DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

"DCS Read Short Response, 1 Byte Returned" (DCSRR1-S), which is defined in Data Type (DT, 10 0001b), is always used in a Short Packet (SPa) from the display module to the MCU. "DCS Read Short Response, 1 Byte Returned (DCSRR1-S) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Short Packet (SPa) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 10 0001b
- Packet Data (PD)
  - ✧ Data 0: 45hex
  - ✧ Data 1: 00hex (Always)
- Error Correction Code (ECC)

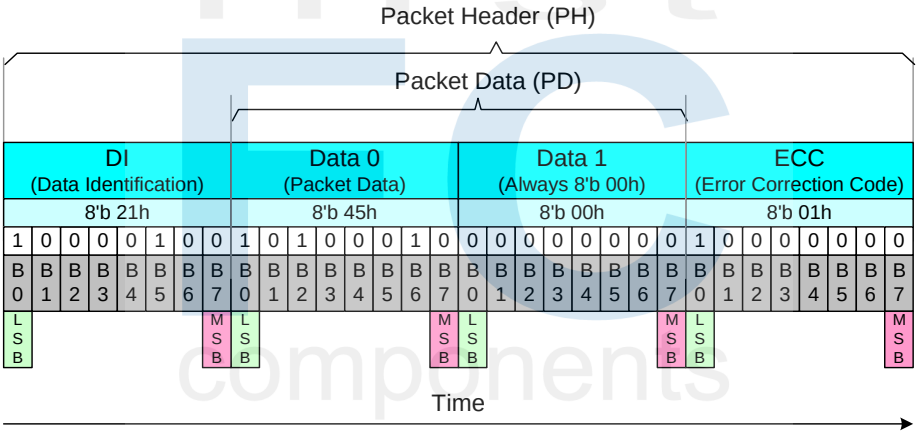


Figure 74: DCS Read Short Response, 1 Byte Returned (DCSRR1-S) - Example

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4.1.3.2.2.5. DCS Read Short Response, 2 Bytes Returned (DCSRR2-S)

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S), which is defined in Data Type (DT, 10 0010b), is always used in a Short Packet (SPa) from the display module to the MCU. "DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Short Packet (SPa) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 10 0010b
- Packet Data (PD)
  - ✧ Data 0: 45hex
  - ✧ Data 1: 32hex
- Error Correction Code (ECC)

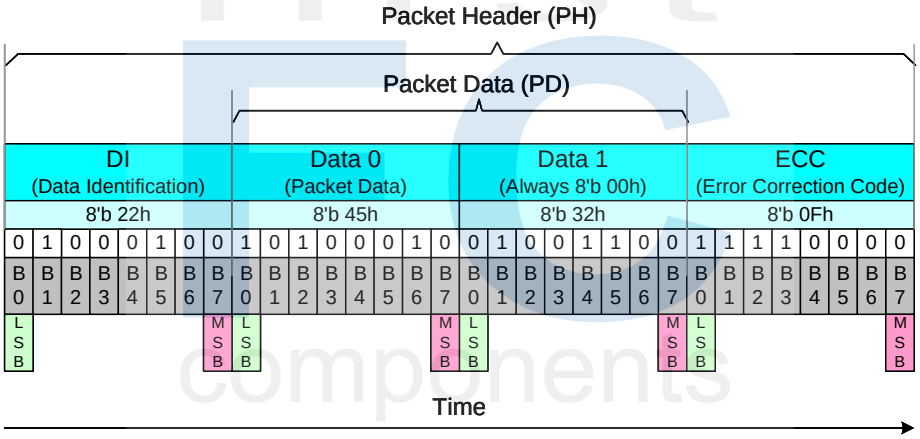


Figure 75: DCS Read Short Response, 2 Bytes Returned (DCSRR2-S) - Example

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4.1.3.3. Communication Sequences

4.1.3.3.1. General

The communication sequences can be done on interface or packet levels between the MCU and the display module. See sections “4.1.2 Interface Level Communication” and “4.1.3 Packet Level Communication”. This communication sequence description is for DSI data lanes (D3P/N, D2P/N, D1P/N and D0P/N), and it is assumed that the needed low level communication is done on DSI Clock lane (CLKP/N) automatically. See the section “4.1.2.2 DSI CLK Lanes”. Functions of the interface level communication are described in the following table.

Table 16: Interface Level Communication

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop State
	LPDT	Low Power Data Transmission
	ULPS	Ultra-Low Power State
	RAR	Remote Application Reset
	ACK	Acknowledge (No Error)
	BTA	Bus Turnaround
High Speed	HSDT	High speed Data Transmission

Functions of the packet level communication are described in the following table.

Table 17: Packet Level Communication for MCU-sourced Packets

Interface Mode	Abbreviation	Packet Size	Interface Action Description
MCU	VSS	Short Packet	Sync Event, V Sync Start
	VSE	Short Packet	Sync Event, V Sync End
	HSS	Short Packet	Sync Event, H Sync Start
	HSE	Short Packet	Sync Event, H Sync End
	EoTP	Short Packet	End of Transmission Packet (EoTP) Note1
	CMOFF	Short Packet	Color Mode Off Command
	CMON	Short Packet	Color Mode On Command
	SDNP	Short Packet	Shut Down Peripheral Command
	TONP	Short Packet	Turn On Peripheral Command
	GENWN-S	Short Packet	Generic Short WRITE, no parameters
	GENW1-S	Short Packet	Generic Short WRITE, 1 parameters
	GENW2-S	Short Packet	Generic Short WRITE, 2 parameters
	GENRN-S	Short Packet	Generic Short READ, no parameters
	GENR1-S	Short Packet	Generic Short READ, 1 parameters
	GENR2-S	Short Packet	Generic Short READ, 2 parameters
	DCSWN-S	Short Packet	DCS Write, No Parameter
	DCSW1-S	Short Packet	DCS Write, 1 Parameter
	DCSRN-S	Short Packet	DCS Read, No Parameter
	SMRPS-S	Short Packet	Set Maximum Return Packet Size
	NP-L	Long Packet	Null Packet, No Data, Note2
	BLK-L	Long Packet	Blanking Packet, no data
	GENW-L	Long Packet	Generic Long Write
	DCSW-L	Long Packet	DCS Write Long
	PKPS16	Long Packet	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format
	PKPS18	Long Packet	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format
	LPKPS18	Long Packet	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format
	PKPS24	Long Packet	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format

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Table 18: Packet Level Communication for Peripheral-sourced packets

Interface Mode	Abbreviation	Packet Size	Interface Action Description
Display Module (ILI9881C-0D)	AwER	Short Packet	Acknowledge with Error Report
	EoTP	Short Packet	End of Transmission Packet
	GENRR1-S	Short Packet	Generic Short READ Response, 1 byte returned
	GENRR2-S	Short Packet	Generic Short READ Response, 2 byte returned
	GENRR-L	Long Packet	Generic Long READ Response
	DCSRR-L	Long Packet	DCS Read Long Response
	DCSRR1-S	Short Packet	DCS Read Short Response, 1 byte returned
	DCSRR2-S	Short Packet	DCS Read Short Response, 2 byte returned

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4.1.3.3.2. Sequences

4.1.3.3.2.1. DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)" is defined in the section "4.1.3.2.1.3 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)" and example sequences on how this packet is used are described in following tables.

Table 19: DCS Write, 1 Parameter Sequence – Example 1

DCS Write, 1 Parameter Sequence – Example 1						
Line	MCU		Information Direction	Display Module (ILI9881C-0D)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 20: DCS Write, 1 Parameter Sequence – Example 2

DCS Write, 1 Parameter Sequence – Example 2						
Line	MCU		Information Direction	Display Module (ILI9881C-0D)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 21: DCS Write, 1 Parameter Sequence – Example 3

DCS Write, 1 Parameter Sequence – Example 3						
Line	MCU		Information Direction	Display Module (ILI9881C-0D)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

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4.1.3.3.2.2. DCS Write, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” is defined in the section “4.1.3.2.1.2 Display Command Set (DCS) Write, No Parameter (DCSWN-S)” and example sequences on how this packet is used are described in following tables.

Table 22: DCS Write, No Parameter Sequence – Example 1

DCS Write, No Parameter Sequence – Example 1						
Line	MCU		Information Direction	Display Module (ILI9881C-0D)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 23: DCS Write, No Parameter Sequence – Example 2

DCS Write, No Parameter Sequence – Example 2						
Line	MCU		Information Direction	Display Module (ILI9881C-0D)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 24: DCS Write, No Parameter Sequence – Example 3

DCS Write, 1 Parameter Sequence – Example 3						
Line	MCU		Information Direction	Display Module (ILI9881C-0D)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

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4.1.3.3.2.3. DCS Write Long Sequence

A Long Packet (LPa) of "Display Command Set (DCS) Write Long (DCSW-L)" is defined in the section "4.1.3.2.1.4 Display Command Set (DCS) Write Long (DCSW-L)" and example sequences on how this packet is used are described in following tables.

Table 25: DCS Write Long Sequence – Example 1

DCS Write Long Sequence – Example 1						
Line	MCU		Information Direction	Display Module (ILI9881C-0D)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 26: DCS Write Long Sequence – Example 2

DCS Write Long Sequence – Example 2						
Line	MCU		Information Direction	Display Module (ILI9881C-0D)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 27: DCS Write Long Sequence – Example 3

DCS Write Long Sequence – Example 3						
Line	MCU		Information Direction	Display Module (ILI9881C-0D)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

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4.1.3.3.2.4. DCS Read, No Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Read, No Parameter (DCSRN-S)" is defined in the section "4.1.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)" and example sequences on how this packet is used are described in following tables.

Table 28: DCS Read, No Parameter Sequence – Example 1

DCS Read, No Parameter Sequence – Example 1						
Line	MCU		Information Direction	Display Module (ILI9881C-0D)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	SMRPS-S	HSDT	→	--	--	Defined how many data byte is wanted to read : 1 byte
3	DCSRN-S	HSDT	→	--	--	Wanted to get a response ID1 (DAh)
4	EoTP	HSDT	→	--	--	End of Transmission Packet
5	--	LP-11	→	--	--	
6	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
7	--	--	←	LP-11	--	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is Corrected by ECC → Go to Line 19
8						
9	--	--	←	LPDT	DCSRR1-S	Response 1 byte return
10	--	--	←	LP-11	--	
11	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
12	--	LP-11	→	--	--	End
13						
14	--	--	←	LPDT	AwER	Error Report
15	--	--	←	LP-11	--	
16	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
17	--	LP-11	→	--	--	End
18						
19	--	--	←	LPDT	DCSRR1-S	Response 1 byte return
20	--	--	←	LPDT	AwER	Error Report (Error is corrected by ECC)
21			←	LP-11	--	
22	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
23	--	LP-11	→	--	--	End

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Table 29: DCS Read, No Parameter Sequence – Example 2

DCS Read, No Parameter Sequence – Example 2						
Line	MCU		Information Direction	Display Module (ILI9881C-0D)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	SMRPS-S	HSDT	→	--	--	Defined how many data byte is wanted to read : 200 bytes
3	DCSRN-S	HSDT	→	--	--	Wanted to get a response
4	EoTP	HSDT	→	--	--	End of Transmission Packet
5	--	LP-11	→	--	--	
6	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
7	--	--	←	LP-11	--	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is Corrected by ECC → Go to Line 19
8						
9	--	--	←	LPDT	DCSRR-L	Response 200 byte return
10	--	--	←	LP-11	--	
11	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
12	--	LP-11	→	--	--	End
13						
14	--	--	←	LPDT	AwER	Error Report
15	--	--	←	LP-11	--	
16	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
17	--	LP-11	→	--	--	End
18						
19	--	--	←	LPDT	DCSRR-S	Response 200 byte return
20	--	--	←	LPDT	AwER	Error Report (Error is corrected by ECC)
21			←	LP-11	--	
22	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
23	--	LP-11	→	--	--	End

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4.1.3.3.2.5. Null Packet, No Data Sequence

A Long Packet (LPa) of "Null Packet, No Data (NP-L)" is defined in the section "4.1.3.2.1.6 Null Packet, No Data (NP-L)", and an example sequence on how this packet is used is described in the following table.

Table 30: Null Packet, No Data Sequence - Example

Null Packet, No Data Sequence – Example						
Line	MCU		Information Direction	Display Module (ILI9881C-0D)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	NP-L	HSDT	→	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

4.1.3.3.2.6. End of Transmission Packet

A Short Packet (SPa) of "End of Transmission (EoTP)" is defined in the section "4.1.3.2.1.7 End of Transmission Packet (EoTP)", and an example sequence on how this packet is used is described in the following table.

Table 31: End of Transmission Packet – Example

End of Transmission Packet – Example						
Line	MCU		Information Direction	Display Module (ILI9881C-0D)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	NP-L	HSDT	→	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

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4.1.3.4. 16 bit / pixel Writing

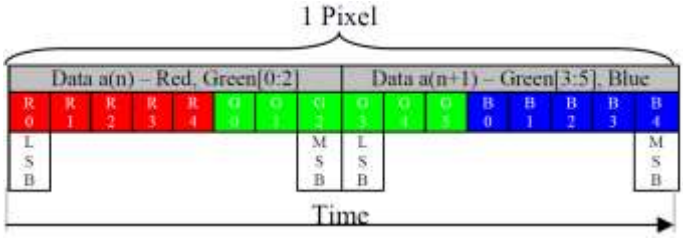


Figure 76: One Pixel Bit and Write Color Orders

The MCU can send to the display module a following packet.

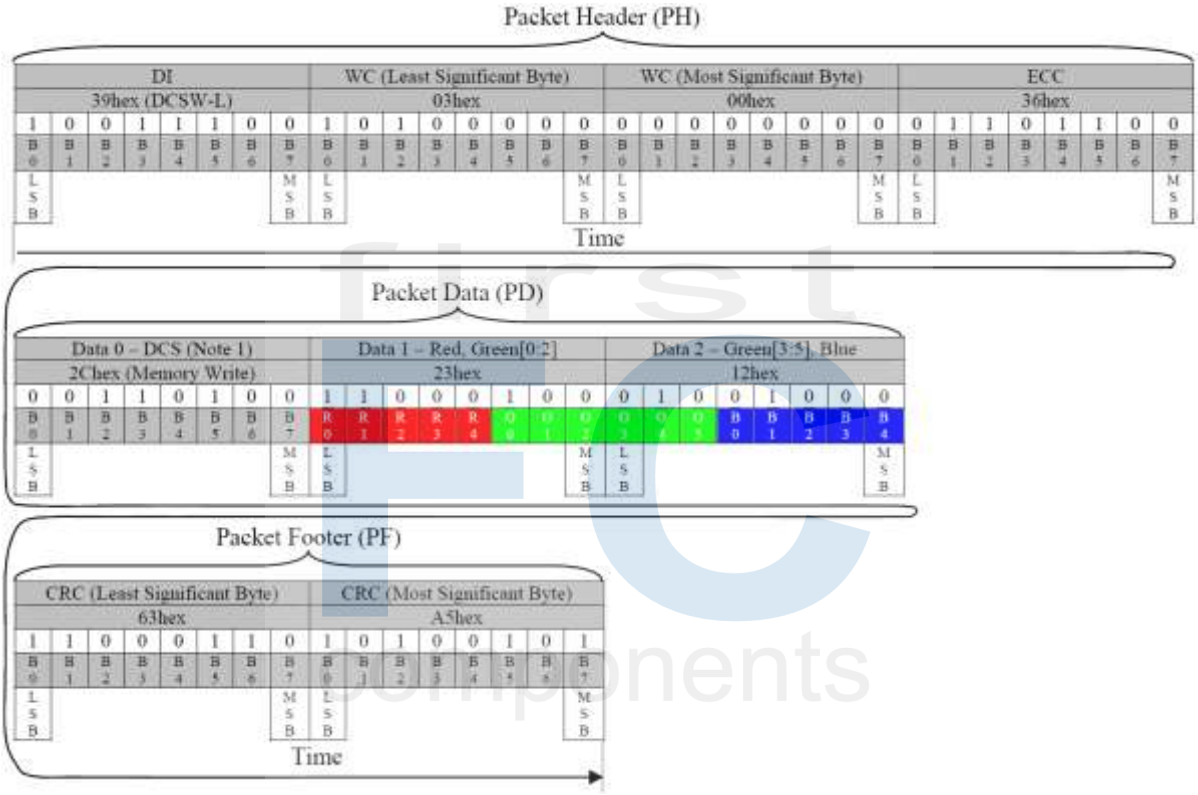


Figure 77: One Pixel Write (DCSW-L) – Example 1

Notes:

1. Memory Write (2Ch) or Memory Write Continue (3Ch)

2. It is possible that one pixel information is split in one different packets which are ending and starting as follows: RG – GB (2 packets)

3. Packet can include several pixels (Not only one pixel as in this example)

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Figure 78: Red / Green [0:2] Subpixel Write (DCSW1-S) – Example 2

Note: *DCS (Data 0) can also be "Memory Write" (2Ch) command*

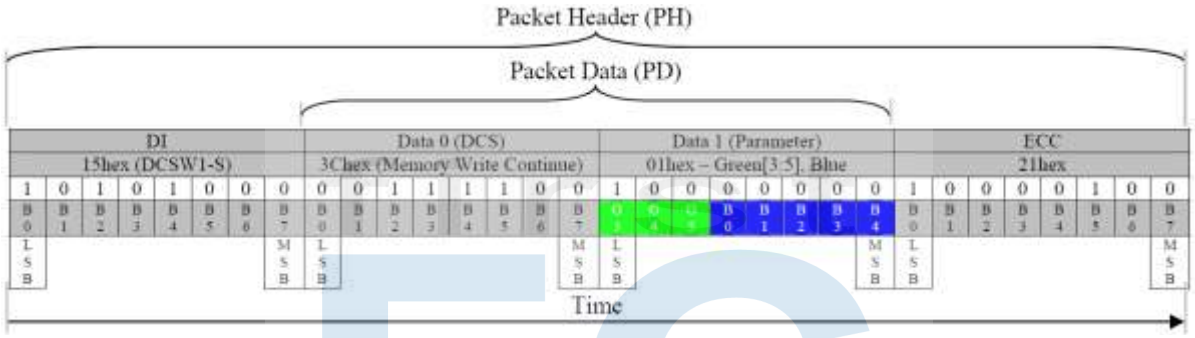


Figure 79: Green [3:5] / Blue Subpixel Write (DCSW1-S) – Example 3

Notes:

1. DCS (Data 0) cannot be "Memory Write" (2Ch) command. It must always be "Memory Write Continue" (3Ch)

2. Previous data byte was R[0:4]G[0:2]

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4.1.3.5. 24 bit/pixel Writing

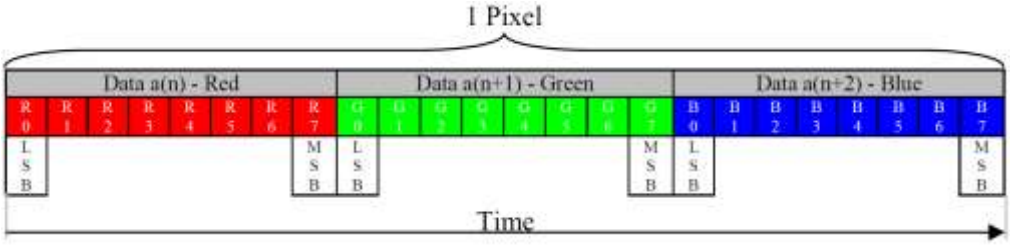


Figure 80: One Pixel Bit and Color Write Orders

The MCU can send to the display module a following packet.

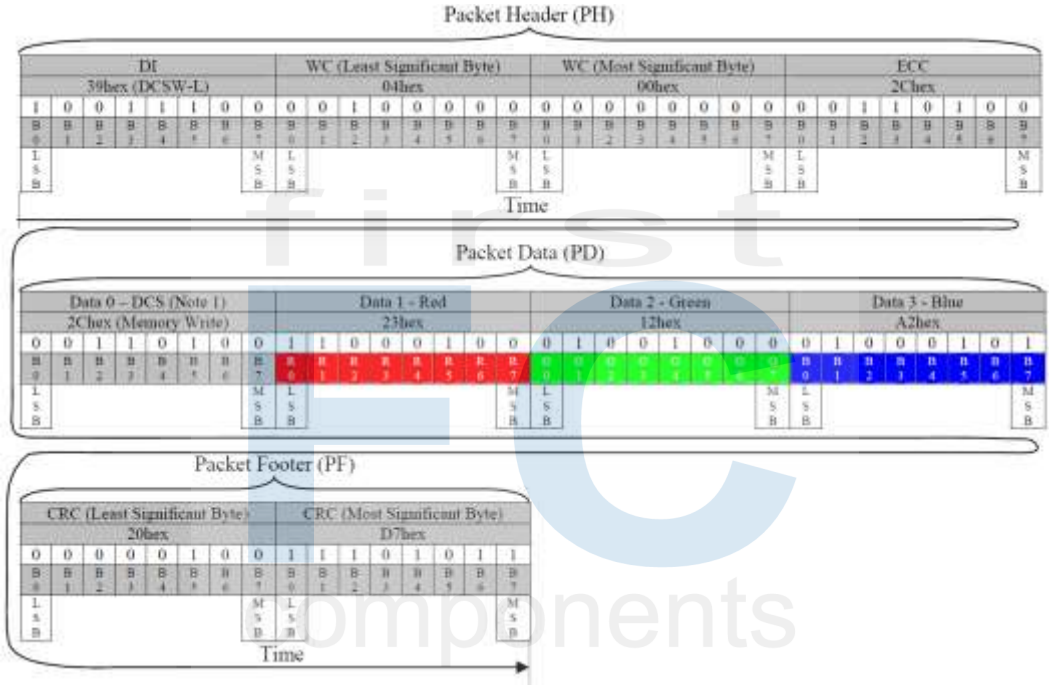


Figure 81: One Pixel Write (DCSW-L) – Example

Notes:

1. Memory Write (2Ch) or Memory Write Continue (3Ch)

2. It is possible that one pixel information is split in two or three different packets which are ending and starting as follows:

- *R – GB (2 packets)*
- *RG – B (2 packets)*
- *R – G – B (3 packets)*

3. Packet can include several pixels (Not only one pixel as in this example)

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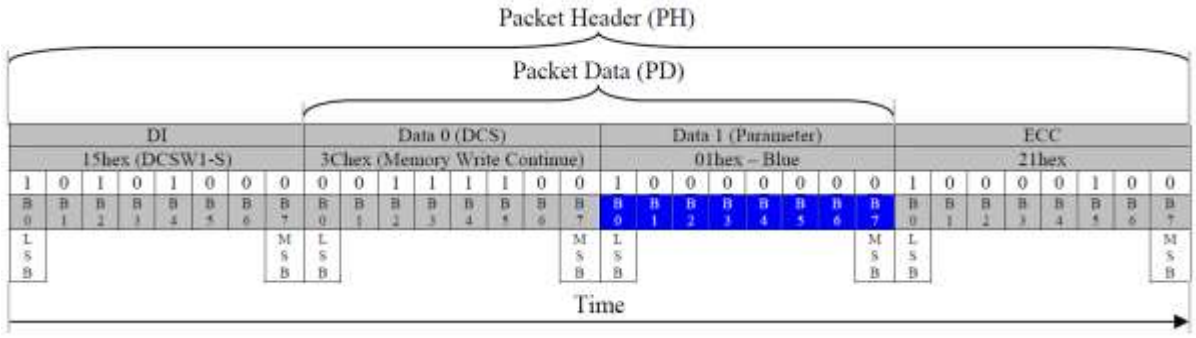


Figure 82: Blue Subpixel Write (DCSW1-S) – Example 2

Notes:

1. DCS (Data 0) cannot be "Memory Write" (2Ch) command. It must always be "Memory Write Continue" (3Ch)

2. Previous data byte was G[0:7]

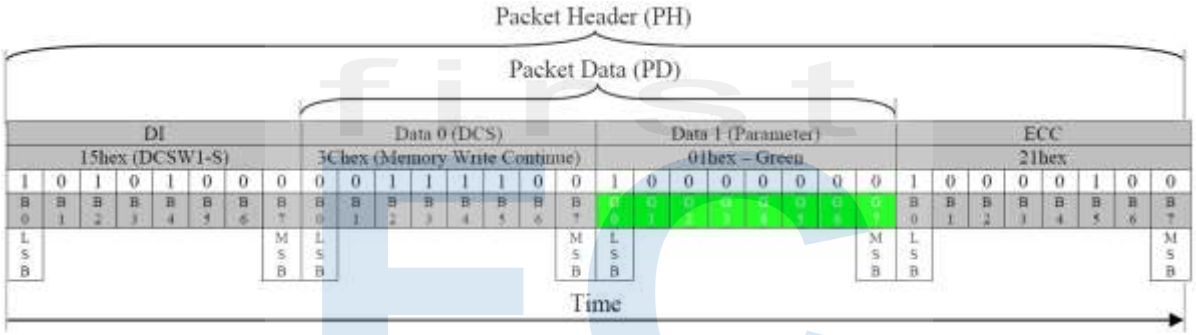


Figure 83: Green Subpixel Write (DCSW1-S) – Example 3

Notes:

1. DCS (Data 0) cannot be "Memory Write" (2Ch) command. It must always be "Memory Write Continue" (3Ch)

2. Previous data byte was R[0:7]

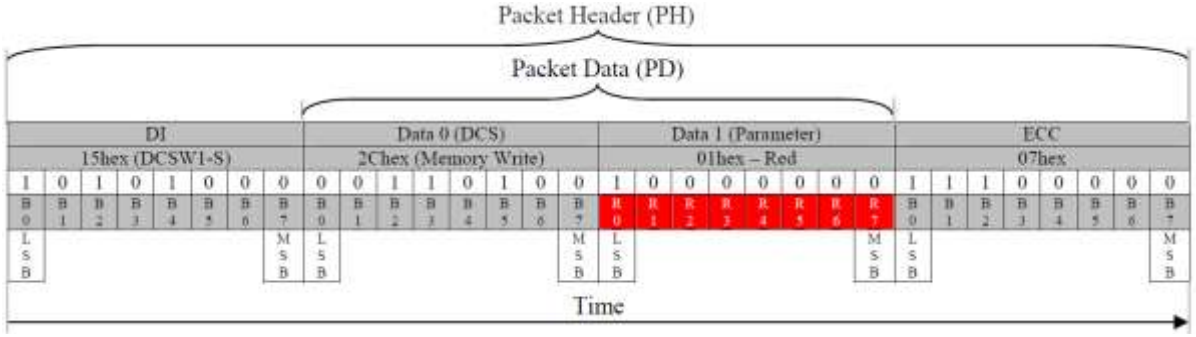


Figure 84: Red Subpixel Write (DCSW1-S) – Example 4

Notes:

1. DCS (Data 0) can also be "Memory Write Continue" (3Ch) command

2. Previous data byte was B[0:7]

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4.2. Display Data Format

4.2.1. DSI Transmission Data Format

4.2.1.1. 16-bit per Pixel, Long Packet, Data Type 00 1110 (0Eh)

Packed Pixel Stream 16-Bit Format is a Long Packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is red (5 bits), green (6 bits), and blue (5 bits), in that order. Note that the Green component is split across two bytes. Within a color component, the LSB is sent first, the MSB last. With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, the ILI9881C-0D has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifice.

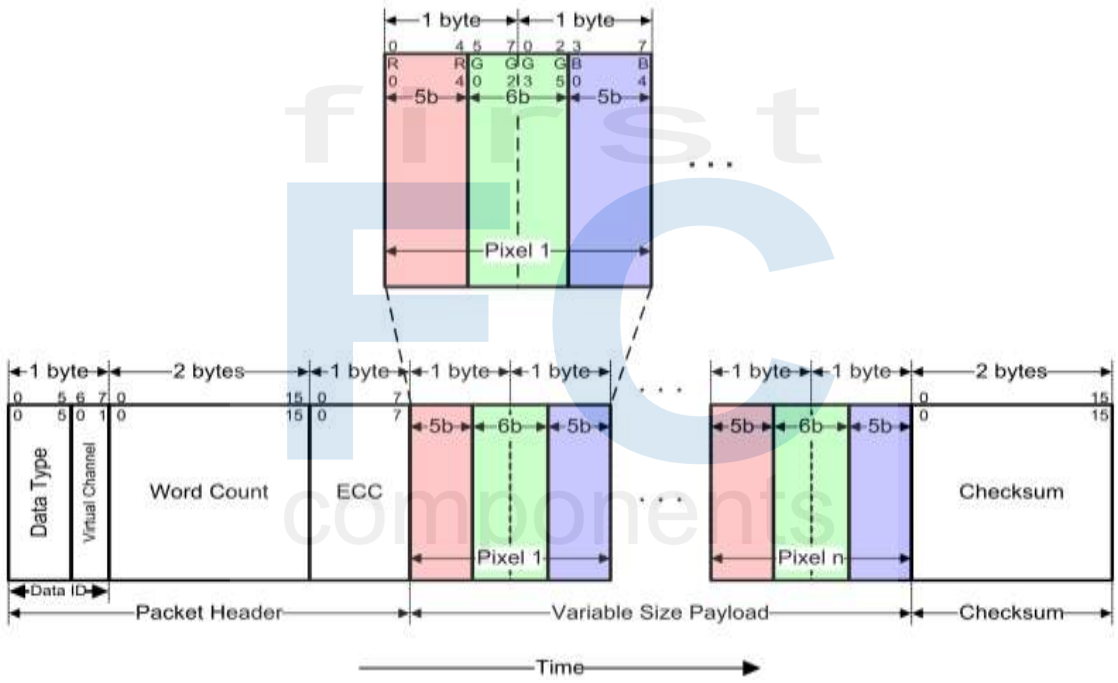


Figure 85: 16-bit per Pixel, Data Type 00 1110 (0Eh)

4.2.1.2. 18-bit per Pixel, Long Packet, Data Type = 01 1110 (1Eh)

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes, and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional filled pixels at the end of the display line to make the transmitted width a

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multiple of four pixels. The receiving peripheral shall not display the filled pixels when refreshing the display device. For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission. With this format, the total line width (displayed and non-displayed pixels) should be a multiple of four pixels (nine bytes).

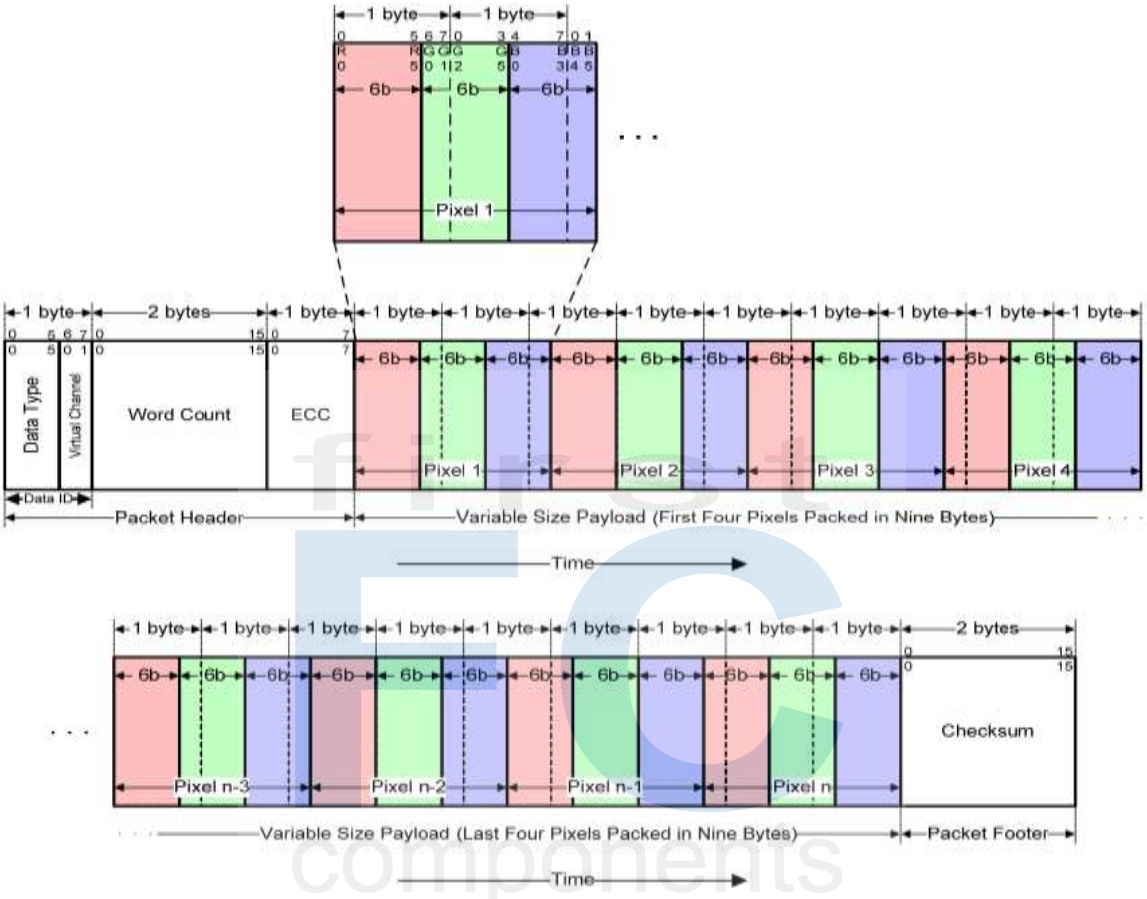


Figure 86: 18-bit per Pixel, Data Type = 01 1110 (1Eh)

4.2.1.3. 18-bit per Pixel, Long Packet, Data Type = 10 1110 (2Eh)

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed and non-displayed pixels) should be a multiple of three bytes.

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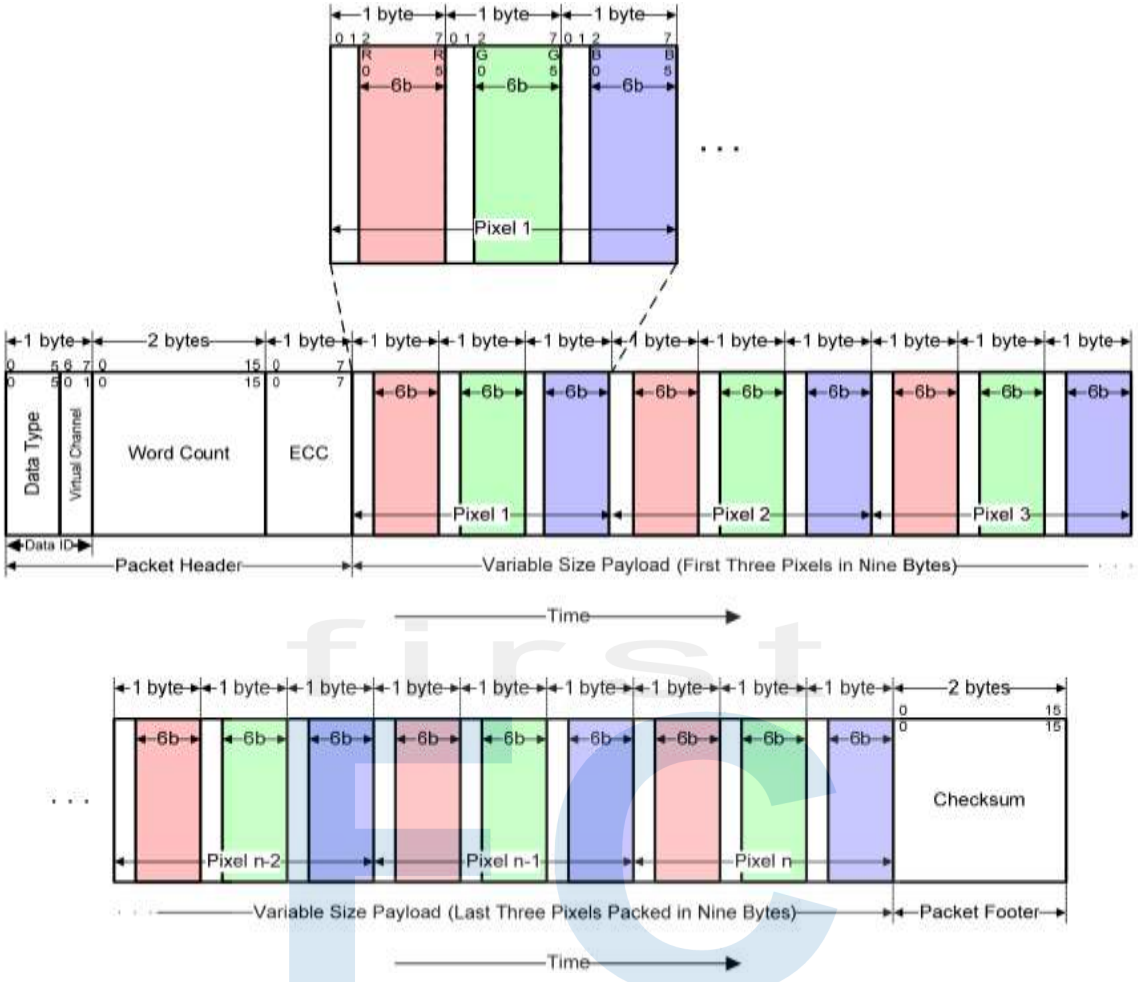


Figure 87: 18-bit per Pixel, Data Type = 10 1110 (2Eh)

4.2.1.4. 24-bit per Pixel, Long Packet, Data Type = 11 1110 (3Eh)

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed and non-displayed pixels) should be a multiple of three bytes.

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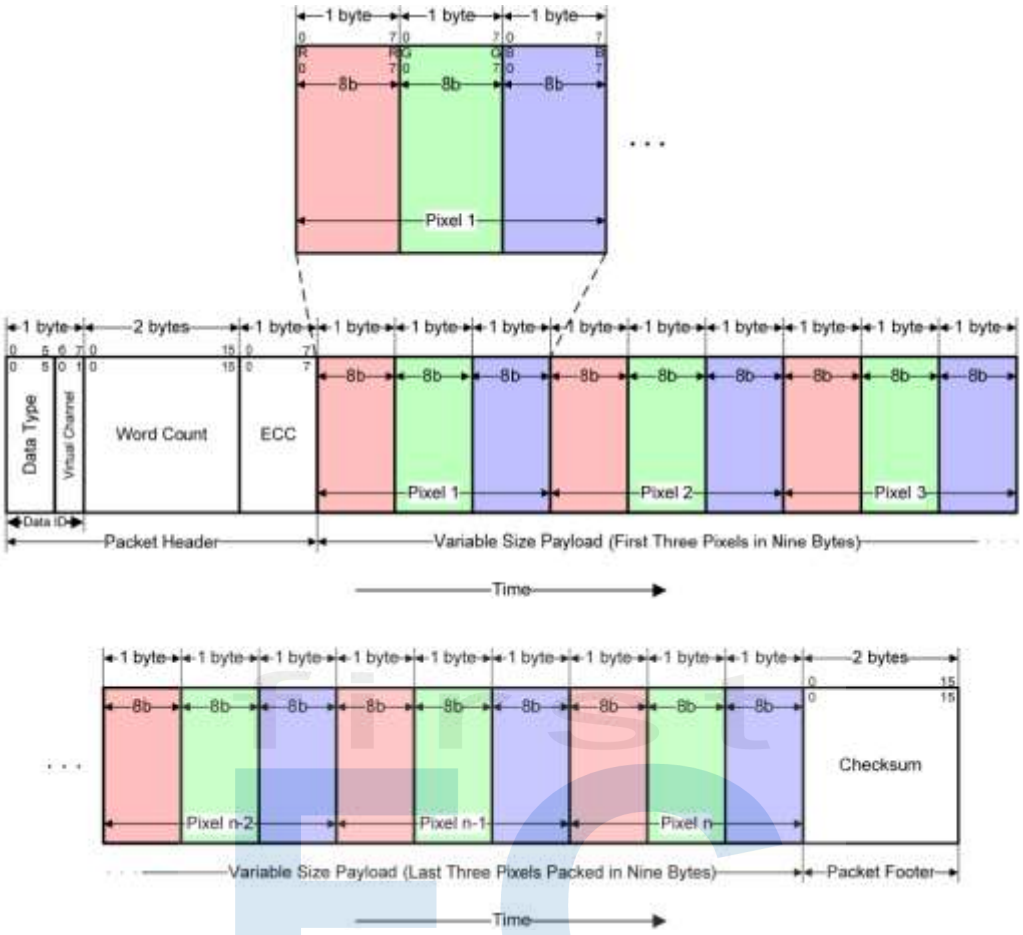


Figure 88: 24-bit per Pixel, Data Type = 11 1110 (3Eh)

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4.2.2. 16/18-bit Color Data Mapping to 24-bit Pixel Data Operation

Table 32 below lists settings for 24-bit data mapping. Set the EPF[1:0] bits function, which defines three types of data formats for 24-bit data (pixel data r, g, b) mapping.

Table 32: 16/18-bit Color Data Mapping to 24-bit Pixel Data Operation

EPF[1:0]	Expand 16-bit color data (R,G,B) to 24-bit subpixel data (r, g, b)	Expand 18-bit color data (R,G,B) to 24-bit subpixel data (r, g, b)
00	0 is written to the LSB. 8 bits subpixel, data r [7:0] = {16-bit color data R [4:0], 3'h0} 8 bits subpixel, data g [7:0] = {16-bit color data G [5:0], 2'h0} 8 bits subpixel, data b [7:0] = {16-bit color data B [4:0], 3'h0} (Note3): that the data are converted as follows. 16-bit color data R [4:0] = 5'h1F, G [5:0] = 6'h3F, B [4:0] = 5'h1F → 24-bit pixel data r, g, b [7:0] = 24'hFFFFFF	0 is written to the LSB. 8 bits subpixel, data r [7:0] = {18-bit color data R [5:0], 2'h0} 8 bits subpixel, data g [7:0] = {18-bit color data G [5:0], 2'h0} 8 bits subpixel, data b [7:0] = {18-bit color data B [5:0], 2'h0} (Note1): that the data are converted as follows. 18-bit color data R [5:0] = 6'h3F, G [5:0] = 6'h3F ,B [5:0] = 6'h3F → 24-bit pixel data r, g, b [7:0] = 24'hFFFFFF
01	1 is written to the LSB. 8 bits subpixel, data r [7:0] = {16-bit color data R [4:0], 3'h7} 8 bits subpixel, data g [7:0] = {16-bit color data G [5:0], 2'h3} 8 bits subpixel, data b [7:0] = {16-bit color data B [4:0], 3'h7} (Note4): that the data are converted as follows. 16-bit color data R [4:0] = 5'h0, G [5:0] = 6'h0, B [4:0] = 5'h0 →24-bit pixel data r, g, b [7:0] = 24'h000000	1 is written to the LSB. 8 bits subpixel, data r [7:0] = {18-bit color data R [5:0], 2'h3} 8 bits subpixel, data g [7:0] = {18-bit color data G [5:0], 2'h3} 8 bits subpixel, data b [7:0] = {18-bit color data B [5:0], 2'h3} (Note2): that the data are converted as follows. 18-bit color data R [5:0] = 6'h0, G [5:0] = 6'h0, B [5:0] = 6'h0 →24-bit pixel data r, g, b [7:0] = 24'h000000
10	The MSB value is written to the LSB. 8 bits subpixel, data r [7:0] = {16-bit color data R [4:0], R [4:2]} 8 bits subpixel, data g [7:0] = {16-bit color data G [5:0], G [5:4]} 8 bits subpixel, data b [7:0] = {16-bit color data B [4:0], B [4:2]}	The MSB value is written to the LSB. 8 bits subpixel, data r [7:0] = {18-bit color data R [5:0], R [5:4]} 8 bits subpixel, data g [7:0] = {18-bit color data G [5:0], G [5:4]} 8 bits subpixel, data b [7:0] = {18-bit color data B [5:0], B [5:4]}
11	Same as setting "EPF [1:0] = 10"	Same as setting "EPF [1:0] = 10"

	Display image data (24 bits)																							
	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
24-bit	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
18-bit EPF[1:0]=00 (Note 1)	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	0	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	0	0	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	0	0
18-bit EPF[1:0]=01 (Note 2)	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	1	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	1	1	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	1	1
18-bit EPF[1:0]=10	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	R[5]	R[4]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	G[5]	G[4]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	B[5]	B[4]
16-bit EPF[1:0]=00 (Note 3)	R[4]	R[3]	R[2]	R[1]	R[0]	0	0	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	0	0	B[4]	B[3]	B[2]	B[1]	B[0]	0	0	0
16-bit EPF[1:0]=01 (Note 4)	R[4]	R[3]	R[2]	R[1]	R[0]	1	1	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	1	1	B[4]	B[3]	B[2]	B[1]	B[0]	1	1	1
16-bit EPF[1:0]=10	R[4]	R[3]	R[2]	R[1]	R[0]	R[4]	R[3]	R[2]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	G[5]	G[4]	B[4]	B[3]	B[2]	B[1]	B[0]	B[4]	B[3]	B[2]

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Example1: 16-bit data mapping to 24-bit, EPF[1:0] = 10

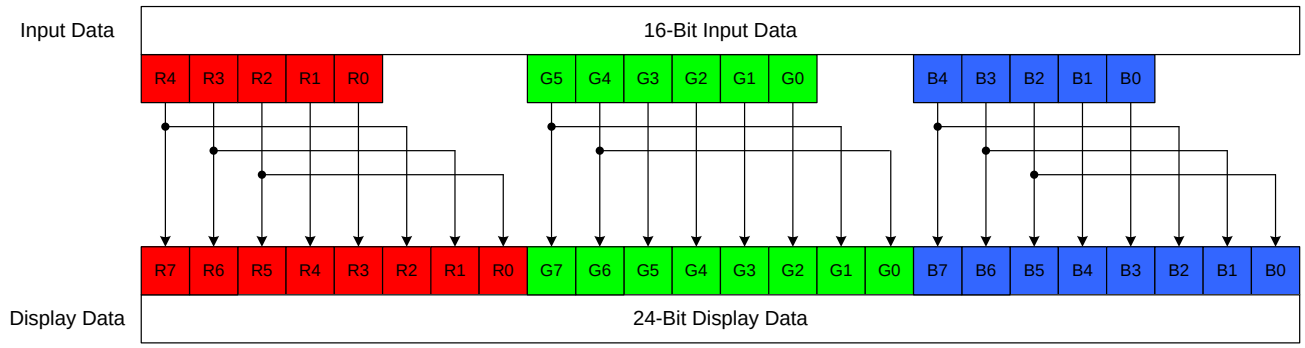


Figure 89: EPF[1:0] = 10, 16-bit Data Mapping to 24-bit

Example2: 18-bit data mapping to 24-bit, EPF[1:0] = 10

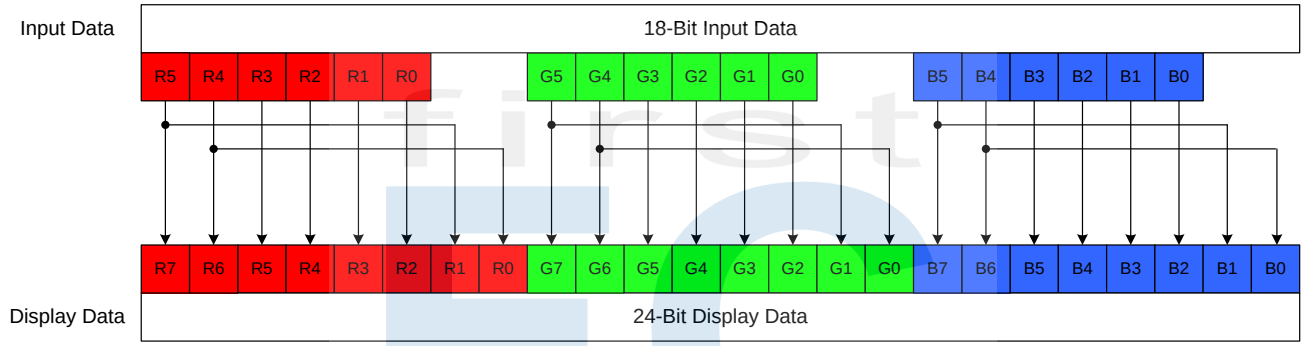


Figure 90: EPF[1:0] = 10, 18-bit Data Mapping to 24-bit

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5. Command

5.1. Command Flow

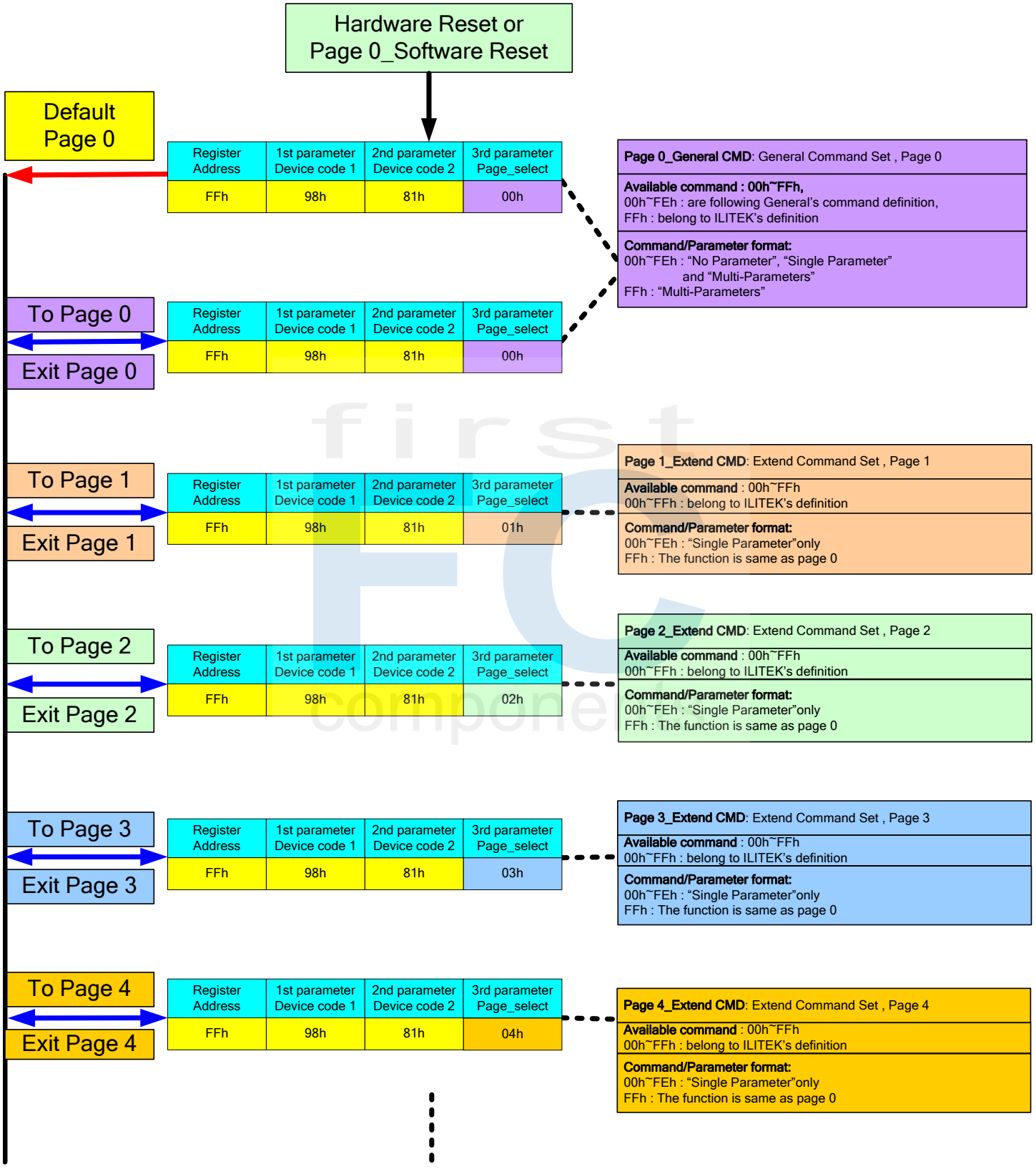


Figure 91: Command Flow

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5.2. Command List

5.2.1. Page 0 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P0	00h	-	W	NOP	No Argument								-	-
P0	01h	-	W	Software Reset	No Argument								-	-
P0	05h	1st	R	Read Number of the Errors on DSI	P[7:0]								00h	-
P0	09h	1st	R	Read Display Status	D31	0	0	0	0	D26	0	D24	00h	-
		2nd	R		D23	0	0	0	D19	0	D17	D16	01h	-
		3rd	R		0	0	0	D12	D11	D10	D9	D8	00h	-
		4th	R		D7	D6	D5	0	0	0	0	D0	00h	-
P0	0Ah	1st	R	Read Display Power Mode	D7	D6	0	D4	D3	D2	0	0	08h	-
P0	0Bh	1st	R	Read Display MADCTL	0	0	0	0	D3	0	D1	D0	00h	-
P0	0Ch	1st	R	Read Pixel Format	0	0	0	0	0	D2	D1	D0	07h	
P0	0Dh	1st	R	Read Display Mode	0	0	0	D4	D3	D2	D1	D0	00h	-
P0	0Eh	1st	R	Read Display signal Mode	D7	D6	0	0	0	0	0	D0	00h	-
P0	0Fh	1st	R	Read Display Self-Diagnostic Result	D7	D6	0	0	0	0	0	D0	00h	-
P0	10h	-	W	Sleep In	No Argument								-	-
P0	11h	-	W	Sleep Out	No Argument								-	-
P0	13h	-	W	Normal Display Mode On	No Argument								-	-
P0	22h	-	W	All Pixel Off	No Argument								-	-
P0	23h	-	W	All Pixel On	No Argument								-	-
P0	26h	1st	W	Gamma Curve Set	0	0	0	0	GC[3:0]				01h	-
P0	28h	-	W	Display Off	No Argument								-	-
P0	29h	-	W	Display ON	No Argument								-	-
P0	2Ch	Nth	W	Memory Write	-								-	-
P0	34h	-	W	TE OFF	No Argument								-	-
P0	35h	1st	W	TE ON	0	0	0	0	0	0	0	M	00h	-
P0	36h	1st	W	Memory Access	0	0	0	0	BGR	0	SS	GS	00h	-
P0	38h	-	W	Idle Mode Off	No Argument								-	-
P0	39h	-	W	Idle Mode On	No Argument								-	-
P0	3Ah	1st	W	Interface Pixel Format	0	0	0	0	0	DBI[2:0]			07h	-
P0	3Ch	Nth	W	Memory Write Continue	-								-	-
P0	44h	1st	W	Set tear scan line	0	0	0	0	0	TE_LINE[10:8]			00h	-
		2nd			TE_LINE[7:0]								00h	-
P0	45h	1st	R	Get tear scan line	0	0	0	0	0	TE_LINE[10:8]			00h	-
		2nd			TE_LINE[7:0]								00h	-
P0	51h	1st	W	Write Display Brightness	0	0	0	0	DBV[11:8]				00h	-
		2nd			DBV[7:0]								00h	-
P0	52h	1st	R	Read Display Brightness Value	0	0	0	0	DBV[11:8]				00h	-
		2nd			DBV[7:0]								00h	-
P0	53h	1st	W	Write CTRL Display	0	0	BCTRL	0	DD	BL	0	0	00h	-
P0	54h	1st	R	Read CTRL Display	0	0	BCTRL	0	DD	BL	0	0	00h	-
P0	55h	1st	W	Write Power Save	PWRSAVE[7:0]								00h	-
P0	56h	1st	R	Read Power Save	PWRSAVE[7:0]								00h	-
P0	59h	-	W	Stop Transition	No Argument								-	-
P0	5Eh	1st	W	Write CABC Minimum Brightness	0	0	0	0	CMB[11:8]				00h	-
		2nd			CMB[7:0]								00h	
P0	5Fh	1st	R	Read CABC Minimum Brightness	0	0	0	0	CMB[11:8]				00h	-
		2nd			CMB[7:0]								00h	
P0	68h	1st	W	Set Transition Time	TT_STP[7:0]								00h	-
		2nd			ST_TIM[7:0]								00h	-
P0	69h	1st	R	Get Transition Time	TT_STP[7:0]								00h	-
		2nd			ST_TIM[7:0]								00h	-

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Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P0	80h	1st	W	Write Idle Mode	0	0	0	0	0	R	G	B	07h	-
P0	81h	1st	R	Read Idle Mode Color	0	0	0	0	0	R	G	B	07h	-
P0	A1h	1st	R	Read the DDB from the provided location	SID[7:0]								00h	1
		2nd			SID[15:8]								00h	1
		3rd			MRID[7:0]								00h	1
		4th			MRID[15:8]								00h	1
		5th			1	1	1	1	1	1	1	1	FFh	-
P0	A8h	1st	R	Continue reading the DDB from the last read location	D1[7:0]								00h	-
		2nd			D2[7:0]								00h	-
		:			:								00h	-
		nth			Dn[7:0]								00h	-
P0	AAh	1st	R	Read First Checksum	FCS[7:0]								00h	-
P0	AFh	1st	R	Read Continue Checksum	CCS[7:0]								00h	-
P0	DAh	1st	R	Read ID1	ID1[7:0]								00h	3
P0	DBh	1st	R	Read ID2	ID2[6:0]								00h	3
P0	DCh	1st	R	Read ID3	ID3[7:0]								00h	3
P0	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	0	1	81h	-
		3rd	W		PAGE[7:0]								00h	-

Notes:

1. Undefined commands are treated as NOP (00h) command.

2. Commands 10h, 13h, 22h, 23h, 26h, 28h, 29h, 36h, 38h, 39h, 51h, 53h, 55h, 5Eh,68h and 80h are updated during V-SYNC when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Commands 05h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, 45h, 52h, 54h, 56h, 5Fh, 69h, 81h, A1h, A8h of these commands is updated immediately both in Sleep In mode and Sleep Out mode.

first FC components

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5.2.2. Page 1 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P1	00h	1st	R	Read ID4	ID4[23:16]								98h	-
P1	01h	1st	R		ID4[15:8]								81h	-
P1	02h	1st	R		ID4[7:0]								1Ch	-
P1	22h	1st	W/R	Set Panel Operation Mode and Data Complement Setting	0	0	EPF[1:0]		BGR_PANEL	REV_PANEL	SS_PANEL	GS_PANEL	30h	1
P1	25h	1st	W/R	Blanking Porch Control	VFP[7:0]								14h	-
P1	26h	1st	W/R		VBP[7:0]								14h	-
P1	29h	1st	W/R	Touch	0	0	0	0	0	0	0	TOUCH_	00h	-
P1	2Eh	1st	W/R	Gate Number	NL[7:0]								C8h	1
P1	31h	1st	W/R	Display Inversion	0	0	0	0	DINV[3:0]				00h	1
P1	34h	1st	W/R	Dithering Enable	0	0	0	0	0	0	0	DITH_EN	00h	1
P1	40h	1st	W/R	Pump Clock Adjustment	0	EXT_CPCK_SEL[1:0		1	0	0	VCL_CLK	VGHL_CL	33h	1
P1	41h	1st	W/R		0	VCL_CLK_SELA[2:0]			0	VCL_CLK_SELB[2:0]			33h	1
P1	42h	1st	W/R		0	VGHL_CLK_SELA[2:0]			0	VGHL_CLK_SELB[2:0]			44h	1
P1	43h	1st	W/R		0	4002_RATIO_FREQA[2:0]			0	4002_RATIO_FREQB[2:0]			55h	1
P1	50h	1st	W/R	Power Control 1	VREG1[7:0]								95h	1
P1	51h	1st	W/R		VREG2[7:0]								95h	1
P1	52h	1st	W/R	VCOM Control 1	0	0	0	0	0	0	0	VCM1[8]	00h	3
P1	53h	1st	W/R		VCM1[7:0]								7Bh	3
P1	54h	1st	W/R		0	0	0	0	0	0	0	VCM2[8]	00h	3
P1	55h	1st	W/R		VCM2[7:0]								7Bh	3
P1	56h	1st	W/R		0	0	0	NVM2	0	0	0	NVM1	00h	-
P1	58h	1st	W/R	Entry Mode Set	LVD_EN	0	0	0	0	0	0	0	00h	1
P1	60h	1st	W/R	Source Timing Adjust	0	0	SDT[5:0]						14h	1
P1	61h	1st	W/R		0	0	CRT[5:0]						00h	1
P1	62h	1st	W/R		0	0	EQT[5:0]						19h	1
P1	63h	1st	W/R		0	0	PCT[5:0]						10h	1
P1	A0h	1st	W/R	Positive Gamma Correction	0	0	VP0[5:0]						00h	1
P1	A1h	1st	W/R		0	VP4[6:0]							0Dh	1
P1	A2h	1st	W/R		0	VP8[6:0]							1Dh	1
P1	A3h	1st	W/R		0	0	VP12[5:0]						11h	1
P1	A4h	1st	W/R		0	0	VP16[5:0]						0Ch	1
P1	A5h	1st	W/R		0	VP24[6:0]							23h	1
P1	A6h	1st	W/R		0	0	VP36[5:0]						17h	1
P1	A7h	1st	W/R		0	0	VP52[5:0]						1Ch	1
P1	A8h	1st	W/R		VP80[7:0]								82h	1
P1	A9h	1st	W/R		0	0	VP111[5:0]						21h	1
P1	AAh	1st	W/R		0	0	VP144[5:0]						2Ah	1
P1	ABh	1st	W/R		VP175[7:0]								6Bh	1
P1	ACh	1st	W/R		0	0	VP203[5:0]						19h	1
P1	ADh	1st	W/R		0	0	VP219[5:0]						14h	1
P1	AEh	1st	W/R		0	VP231[6:0]							45h	1
P1	AFh	1st	W/R		0	0	VP239[5:0]						1Dh	1
P1	B0h	1st	W/R		0	0	VP243[5:0]						23h	1
P1	B1h	1st	W/R		0	VP247[6:0]							52h	1
P1	B2h	1st	W/R		0	VP251[6:0]							63h	1
P1	B3h	1st	W/R		0	0	VP255[5:0]						39h	1
P1	B6h	1st	W/R	Pad Control	IM_SW_EN	IM_SW[2:0]			RS_SW_EN	0	RS_SW[1:0]		00h	1
P1	B7h	1st	W/R		0	0	0	0	0	0	LANSEL_SW_EN	LANSEL_SW	00h	1

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Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default	MTP
Page	Address	Parameter											(hex)	(times)
P1	C0h	1st	W/R	Negative Gamma Correction	0	0	VN0[5:0]						00h	1
P1	C1h	1st	W/R		0	VN4[6:0]							0Dh	1
P1	C2h	1st	W/R		0	VN8[6:0]							1Dh	1
P1	C3h	1st	W/R		0	0	VN12[5:0]						11h	1
P1	C4h	1st	W/R		0	0	VN16[5:0]						0Ch	1
P1	C5h	1st	W/R		0	VN24[6:0]							23h	1
P1	C6h	1st	W/R		0	0	VN36[5:0]						17h	1
P1	C7h	1st	W/R		0	0	VN52[5:0]						1Ch	1
P1	C8h	1st	W/R		VN80[7:0]								82h	1
P1	C9h	1st	W/R		0	0	VN111[5:0]						21h	1
P1	CAh	1st	W/R		0	0	VN144[5:0]						2Ah	1
P1	CBh	1st	W/R		VN175[7:0]								6Bh	1
P1	CCh	1st	W/R		0	0	VN203[5:0]						19h	1
P1	CDh	1st	W/R		0	0	VN219[5:0]						14h	1
P1	CEh	1st	W/R		0	VN231[6:0]							45h	1
P1	CFh	1st	W/R		0	0	VN239[5:0]						1Dh	1
P1	D0h	1st	W/R		0	0	VN243[5:0]						23h	1
P1	D1h	1st	W/R		0	VN247[6:0]							52h	1
P1	D2h	1st	W/R		0	VN251[6:0]							63h	1
P1	D3h	1st	W/R		0	0	VN255[5:0]						39h	1
P1	E0h	1st	W/R	NV Memory Write	PGM_DATA[7:0]								00h	-
P1	E1h	1st	W/R		PGM_ADR[7:0]								00h	-
P1	E2h	1st	W/R		PGM_ADR[15:8]								00h	-
P1	E3h	1st	W/R	NV Memory Protection Key	KEY[23:16]								00h	-
P1	E4h	1st	W/R		KEY[15:8]								00h	-
P1	E5h	1st	W/R		KEY[7:0]								00h	-
P1	E6h	1st	R	NV Memory Status Read	0	ID2_MK[2:0]			0	ID1_MK[2:0]			00h	-
P1	E7h	1st	R		0	0	0	0	0	ID3_MK[2:0]			00h	-
P1	E8h	1st	R		GAMMA_P_MK	GAMMA_N_MK	VCM2_MK[2:0]			VCM1_MK[2:0]			00h	-
P1	E9h	1st	R		OTP_BUSY	0	0	0	0	0	0	0	00h	-
P1	F0h	1st	W/R	Time Stamp	Time_Stamp_Week[7:0]								00h	1
P1	F1h	1st	W/R		Time_Stamp_Year[7:0]								00h	1
P1	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	0	1	81h	-
		3rd	W		PAGE[7:0]								01h	-

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5.2.3. Page 2 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P2	03h	1st	W/R	Dynamic Backlight Control 1	0	TT_STP_MED[2:0]			1	TT_STP_LOW[2:0]			29h	1
P2	04h	1st	W/R		0	ST_TIM_LOW[2:0]			0	TT_STP_HIGH[2:0]			14h	1
P2	05h	1st	W/R		0	ST_TIM_HIGH[2:0]			0	ST_TIM_MED[2:0]			32h	1
P2	06h	1st	W/R	Dynamic Backlight Control 2	0	PWM_DUTY_PRECISION[2:0]			0	LEDPWM_POL	LEDON_POL	LEDON	00h	1
P2	07h	1st	W/R		PWM_DIV[7:0]								0Eh	1
P2	10h	1st	W/R	IIE Function Control	0	0	0	0	0	PRT_EN	SKIN_EN	0	06h	1
P2	11h	1st	W/R		0	AUTO_MEAN	0	0	CN_EN	CN_INV	SHP_EN	0	00h	1
P2	12h	1st	W/R		0	0	0	0	0	0	CN_LV[1:0]		02h	1
P2	13h	1st	W/R		0	0	1	0	SRE_MIDIV_LV[1:0		0	0	20h	1
P2	15h	1st	W/R		RGB_MEAN[7:0]								80h	1
P2	16h	1st	W/R		SRE_HYSTERESIS_EN	0	0	SRE_DIM_EN	SRE_SC_EN	SRE_CE_EN	0	0	1Ch	1
P2	17h	1st	W/R		0	SRE_OFFS[2:0]			0	SRE_DIM_STP[2:0]			01h	1
P2	18h	1st	W/R		SRE_DIM_FRAME[7:0]								08h	1
P2	19h	1st	W/R		SRE_SC_GAIN_ADJ[2:0]			SRE_HYSTERESIS_LIMIT[4:0]					C0h	1
P2	1Ah	1st	W/R	IIE Saturation Enhancement Control 1	0	0	SE_RATIO_L[5:0]						07h	1
P2	1Bh	1st	W/R		0	0	SE_RATIO_M[5:0]						09h	1
P2	1Ch	1st	W/R		0	0	SE_RATIO_H[5:0]						0Ch	1
P2	40h	1st	W/R	IIE Saturation Protection Control	0	0	0	LEVEL0_SR[4:0]					02h	1
P2	41h	1st	W/R		0	0	0	LEVEL1_SR[4:0]					04h	1
P2	42h	1st	W/R		0	0	0	LEVEL2_SR[4:0]					06h	1
P2	43h	1st	W/R		0	0	0	LEVEL3_SR[4:0]					08h	1
P2	44h	1st	W/R		0	0	0	LEVEL4_SR[4:0]					0Ah	1
P2	45h	1st	W/R		0	0	0	LEVEL5_SR[4:0]					0Ch	1
P2	46h	1st	W/R		0	0	0	LEVEL6_SR[4:0]					0Eh	1
P2	47h	1st	W/R		0	0	0	LEVEL7_SR[4:0]					0Eh	1
P2	48h	1st	W/R		0	0	0	LEVEL8_SR[4:0]					0Ch	1
P2	49h	1st	W/R		0	0	0	LEVEL9_SR[4:0]					0Ah	1
P2	4Ah	1st	W/R		0	0	0	LEVEL10_SR[4:0]					08h	1
P2	4Bh	1st	W/R		0	0	0	LEVEL11_SR[4:0]					06h	1
P2	4Ch	1st	W/R		0	0	0	LEVEL12_SR[4:0]					04h	1
P2	4Dh	1st	W/R		0	0	0	LEVEL13_SR[4:0]					03h	1
P2	4Eh	1st	W/R		0	0	0	LEVEL14_SR[4:0]					02h	1
P2	4Fh	1st	W/R		0	0	0	LEVEL15_SR[4:0]					00h	1
P2	5Ah	1st	W/R	IIE Sharpness Enhancement Control	0	0	0	SHP_RATIO[4:0]					18h	1
P2	5Bh	1st	W/R		SHP_THR_H[7:0]								64h	1
P2	5Ch	1st	W/R		SHP_THR_L[7:0]								1Eh	1
P2	60h	1st	W/R	IIE Contrast Enhancement Control	0	0	CN_00[5:0]						0Eh	1
P2	61h	1st	W/R		0	0	CN_01[5:0]						18h	1
P2	62h	1st	W/R		0	0	CN_02[5:0]						24h	1
P2	63h	1st	W/R		0	0	CN_03[5:0]						28h	1
P2	64h	1st	W/R		0	0	CN_04[5:0]						24h	1
P2	65h	1st	W/R		0	0	CN_05[5:0]						18h	1
P2	66h	1st	W/R		0	0	CN_06[5:0]						0Eh	1
P2	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	0	1	81h	-
		3rd	W		PAGE[7:0]								02h	-

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5.2.4. Page 3 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P3	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	0	1	81h	-
		3rd	W		PAGE[7:0]								03h	-

first FC components

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5.2.5. Page 4 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P4	00h	1st	W/R	DSI Lanes Control	MIPI_LANE_SEL	0	0	0	0	0	0	0	80h	1
P4	0Bh	1st	W/R	SSC Function	SSC_DIG_EN	SSC_DIG_STEP[2:0]			0	0	0	0	00h	-
P4	0Eh	1st	W/R		SSC_DIG_CNT[7:0]								00h	-
P4	21h	1st	W/R	Charge-Pump Setting	DMY_PUMP	0	1	1	0	0	0	0	B0h	1
P4	23h	1st	W/R	Idle Mode Frame Rate	RTNB[7:0]								2Dh	1
P4	26h	1st	W/R	Internal SD Timing Control	DET_TOLERANCE_OP[3:0]				0	1	1	0	76h	1
P4	27h	1st	W/R	Touch Synchronization Timing Adjust	TOUCH_OPT[1:0]		VSOD[1:0]		HSOM[1:0]		HFP_HBP_OPT	VS_PW_OPT	00h	1
P4	28h	1st	W/R		HSOD[7:0]								05h	1
P4	29h	1st	W/R		HSOHW[7:0]								19h	1
P4	2Ah	1st	W/R		VS_OUT_EN	HS_OUT_EN	VS_OUT_POL	HS_OUT_POL	0	0	STB_EN	0	F0h	1
P4	2Dh	1st	W/R	BIST Mode Function	FRM_PT[7:0]								FFh	1
P4	2Fh	1st	W/R		0	0	FRM_CYC[1:0]		0	0	0	FRM_EN	00h	1
P4	35h	1st	W/R	Source Timing Setting	0	0	0	1	HZ_OPT	1	1	1	17h	1
P4	3Ah	1st	W/R	Power Saving Control	PS_EN	PCST[6:0]							A4h	1
P4	69h	1st	W/R	Power Control 1	1	CP_VCL_CLP_OPTION_PRE[2:0]			0	1	1	1	D7h	-
P4	6Eh	1st	W/R	Power Control 2	0	DI_PWR_REG	REG1_VRH_CP[5:0]						6Ah	1
P4	6Fh	1st	W/R	Power Control 3	VGLREG_EN_GO	DI_CP_VGH_BH[2:0]			DI_CP_VGL_BL[2:0]			DI_CP_VCL_REG_SEL	34h	1
P4	7Ah	1st	W/R	VREG1/2 Setting	0	0	0	DI_REG_REG1_EN_CAP	0	0	0	0	00h	1
P4	87h	1st	W/R	LVD Function 1	DI_LVD_CTL[3:0]				1	0	1	0	BAh	1
P4	88h	1st	W/R	LVD Function 2	DIS_LVD_CHK	0	0	0	1	0	1	1	8Bh	1
P4	8Bh	1st	W/R	VCOM Control 2	1	1	1	0	DI_VCM_SEL0_E	0	1	1	E3h	1
P4	8Ch	1st	W/R	Power Control 4	0	DI_VCOM_REG_VGLREG[6:0]							03h	1
P4	8Dh	1st	W/R		0	DI_VCOM_CP_VGLCLP[6:0]							14h	1
P4	B2h	1st	W/R	Reload Gamma Setting	RELOAD_GMA_EN	RELOAD_GMA_LINE8_EN	0	1	0	0	0	1	D1h	1
P4	B5h	1st	W/R	Gamma Bias Level	0	0	0	0	0	DI_GMA_GAP[2:0]			02h	1
P4	BBh	1st	W/R	TS_CTRL 1	EN_TEMP_PROCESS	0	CP_VGH_TAP_C[5:0]						1Eh	1
P4	BCh	1st	W/R		0	0	CP_VGH_TAP_L[5:0]						1Eh	1
P4	BDh	1st	W/R		0	0	CP_VGH_TAP_M[5:0]						1Eh	1
P4	BEh	1st	W/R		0	0	CP_VGH_TAP_H[5:0]						1Eh	1
P4	BFh	1st	W/R		VCOM_C[7:0]								4Ch	1
P4	C0h	1st	W/R		VCOM_L[7:0]								4Ch	1
P4	C1h	1st	W/R		VCOM_M[7:0]								4Ch	1
P4	C2h	1st	W/R		VCOM_H[7:0]								4Ch	1
P4	C4h	1st	R	Read VCOM OTP Data	0	0	0	0	0	0	0	OTP_VCM1[8]	00h	-
P4	C5h	1st	R		OTP_VCM1[7:0]								7Bh	-
P4	C6h	1st	R		0	0	0	0	0	0	0	OTP_VCM2[8]	00h	-
P4	C7h	1st	R		OTP_VCM2[7:0]								7Bh	-

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Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P4	C8h	1st	W/R	TS_CTRL 2	TS_TH0[7:0]								00h	-
P4	C9h	1st	W/R		TS_TH1[7:0]								00h	-
P4	CAh	1st	W/R		TS_TH2[7:0]								00h	-
P4	CBh	1st	W/R		TS_TH3[7:0]								00h	-
P4	CCh	1st	W/R		TS_TH0[9:8]		TS_TH1[9:8]		TS_TH2[9:8]		TS_TH3[9:8]		00h	1
P4	CDh	1st	W/R		TS_DEBT_OPT[3:0]				TS_HYST_OPT[3:0]				02h	1
P4	CEh	1st	W/R		EN_TS	VCOM_C [8]	VCOM_L [8]	VCOM_ M[8]	VCOM_ H[8]	1	0	0	04h	1
P4	D7h	1st	W/R	OTP Control	0	0	0	OTP_PA TH	PROG_SEL[1:0]		0	0	1C	-
P4	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	0	1	81h	-
		3rd	W		PAGE[7:0]								04h	-

first FC components

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5.2.6. Page 5 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P5	00h	1st	W	Fine Digital Gamma Control 1	RDIN0[7:0]								00h	-
P5	01h	1st	W		RDIN1[7:0]								00h	-
P5	02h	1st	W		RDIN2[7:0]								00h	-
P5	03h	1st	W		RDIN3[7:0]								00h	-
P5	04h	1st	W		RDIN4[7:0]								00h	-
P5	05h	1st	W		RDIN5[7:0]								00h	-
P5	:	1st	W		:								00h	-
P5	7Ah	1st	W		RDIN122[7:0]								00h	-
P5	7Bh	1st	W		RDIN123[7:0]								00h	-
P5	7Ch	1st	W		RDIN124[7:0]								00h	-
P5	7Dh	1st	W		RDIN125[7:0]								00h	-
P5	7Eh	1st	W		RDIN126[7:0]								00h	-
P5	7Fh	1st	W		RDIN127[7:0]								00h	-
P5	80h	1st	W/R	Digital 3 Gamma Enable	0	0	0	0	0	0	0	EN_3G	00h	-
P5	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	0	1	81h	-
		3rd	W		PAGE[7:0]								05h	-

5.2.7. Page 6 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P6	00h	1st	W	Fine Digital Gamma Control 2	RDIN128[7:0]								00h	-
P6	01h	1st	W		RDIN129[7:0]								00h	-
P6	02h	1st	W		RDIN130[7:0]								00h	-
P6	03h	1st	W		RDIN131[7:0]								00h	-
P6	04h	1st	W		RDIN132[7:0]								00h	-
P6	05h	1st	W		RDIN133[7:0]								00h	-
P6	:	1st	W		:								00h	-
P6	7Ah	1st	W		RDIN250[7:0]								00h	-
P6	7Bh	1st	W		RDIN251[7:0]								00h	-
P6	7Ch	1st	W		RDIN252[7:0]								00h	-
P6	7Dh	1st	W		RDIN253[7:0]								00h	-
P6	7Eh	1st	W		RDIN254[7:0]								00h	-
P6	7Fh	1st	W		RDIN255[7:0]								00h	-
P6	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	0	1	81h	-
		3rd	W		PAGE[7:0]								06h	-

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5.2.8. Page 7 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P7	00h	1st	W	Fine Digital Gamma Control 3	GDIN0[7:0]								00h	-
P7	01h	1st	W		GDIN1[7:0]								00h	-
P7	02h	1st	W		GDIN2[7:0]								00h	-
P7	03h	1st	W		GDIN3[7:0]								00h	-
P7	04h	1st	W		GDIN4[7:0]								00h	-
P7	05h	1st	W		GDIN5[7:0]								00h	-
P7	:	1st	W		:								00h	-
P7	7Ah	1st	W		GDIN122[7:0]								00h	-
P7	7Bh	1st	W		GDIN123[7:0]								00h	-
P7	7Ch	1st	W		GDIN124[7:0]								00h	-
P7	7Dh	1st	W		GDIN125[7:0]								00h	-
P7	7Eh	1st	W		GDIN126[7:0]								00h	-
P7	7Fh	1st	W		GDIN127[7:0]								00h	-
P7	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	0	1	81h	-
		3rd	W		PAGE[7:0]								07h	-

5.2.9. Page 8 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P8	00h	1st	W	Fine Digital Gamma Control 4	GDIN128[7:0]								00h	-
P8	01h	1st	W		GDIN129[7:0]								00h	-
P8	02h	1st	W		GDIN130[7:0]								00h	-
P8	03h	1st	W		GDIN131[7:0]								00h	-
P8	04h	1st	W		GDIN132[7:0]								00h	-
P8	05h	1st	W		GDIN133[7:0]								00h	-
P8	:	1st	W		:								00h	-
P8	7Ah	1st	W		GDIN250[7:0]								00h	-
P8	7Bh	1st	W		GDIN251[7:0]								00h	-
P8	7Ch	1st	W		GDIN252[7:0]								00h	-
P8	7Dh	1st	W		GDIN253[7:0]								00h	-
P8	7Eh	1st	W		GDIN254[7:0]								00h	-
P8	7Fh	1st	W		GDIN255[7:0]								00h	-
P8	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	0	1	81h	-
		3rd	W		PAGE[7:0]								08h	-

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5.2.10. Page 9 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P9	00h	1st	W	Fine Digital Gamma Control 5	BDIN0[7:0]								00h	-
P9	01h	1st	W		BDIN1[7:0]								00h	-
P9	02h	1st	W		BDIN2[7:0]								00h	-
P9	03h	1st	W		BDIN3[7:0]								00h	-
P9	04h	1st	W		BDIN4[7:0]								00h	-
P9	05h	1st	W		BDIN5[7:0]								00h	-
P9	:	1st	W		:								00h	-
P9	7Ah	1st	W		BDIN122[7:0]								00h	-
P9	7Bh	1st	W		BDIN123[7:0]								00h	-
P9	7Ch	1st	W		BDIN124[7:0]								00h	-
P9	7Dh	1st	W		BDIN125[7:0]								00h	-
P9	7Eh	1st	W		BDIN126[7:0]								00h	-
P9	7Fh	1st	W		BDIN127[7:0]								00h	-
P9	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	0	1	81h	-
		3rd	W		PAGE[7:0]								09h	-

5.2.11. Page 10 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P10	00h	1st	W	Fine Digital Gamma Control 6	BDIN128[7:0]								00h	-
P10	01h	1st	W		BDIN129[7:0]								00h	-
P10	02h	1st	W		BDIN130[7:0]								00h	-
P10	03h	1st	W		BDIN131[7:0]								00h	-
P10	04h	1st	W		BDIN132[7:0]								00h	-
P10	05h	1st	W		BDIN133[7:0]								00h	-
P10	:	1st	W		:								00h	-
P10	7Ah	1st	W		BDIN250[7:0]								00h	-
P10	7Bh	1st	W		BDIN251[7:0]								00h	-
P10	7Ch	1st	W		BDIN252[7:0]								00h	-
P10	7Dh	1st	W		BDIN253[7:0]								00h	-
P10	7Eh	1st	W		BDIN254[7:0]								00h	-
P10	7Fh	1st	W		BDIN255[7:0]								00h	-
P10	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	0	1	81h	-
		3rd	W		PAGE[7:0]								0Ah	-

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5.3. Page 0 Command Description

5.3.1. NOP (00h)

<table>
<tr><th colspan="2">Command Page</th><th colspan="10">Page 0</th></tr>
<tr><th>Address</th><th>Parameter</th><th>W/R</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>00h</td><td>-</td><td>W</td><td colspan="9">No Argument</td><td>-</td></tr>
<tr><td>Description</td><td colspan="12">00h: NOP (No Operation).
This command is an empty command. It does not have any effect on the ILI9881C-0D.
However, it can be used to terminate Memory Write or Memory Write Continue as described in RAMWR (Memory Write) and RAMWRC (Memory Write Continue) Commands.</td></tr>
<tr><td>Restriction</td><td colspan="12">None</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"></td></tr>
</table>

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5.3.2. Software Reset (01h)

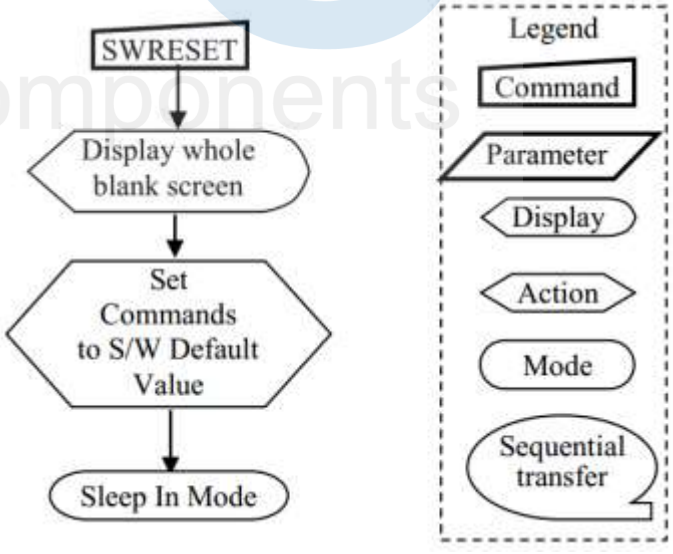
Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
01h	-	W	No Argument								-
Description		01h: SWRESET (Software Reset). When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) The display is blank immediately. *Note: The Frame Memory content is kept or not by this command*									
Restriction		It is necessary to wait 5msec before sending a new command after software reset. The display module loads all factory default values of the display supplier to the registers during this 5msec. If Software Reset is applied during the Sleep Out mode, it will be necessary to wait 120msec for Sleep In sequence before sending the Sleep Out command. The Software Reset Command cannot be sent during the Sleep Out sequence.									
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

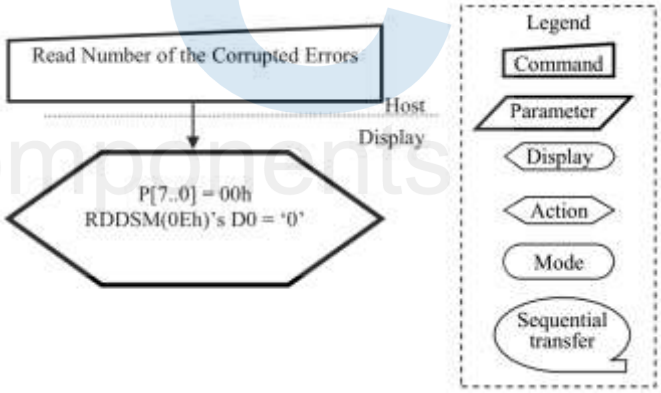
Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart



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5.3.3. Read Number of the Errors on DSI (05h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
05h	1st	R	P[7:0]								00h
Description		05h: RDNUMED (Read Number of the Errors on DSI). The parameter indicates the amount of errors on the DSI. The more detailed description of the bits is below. P[6..0] bits indicate the amount of the error. P[7] is set to 1 if there is overflow with P[6..0] bits. P[7..0] bits are set to 0 (and RDDSM (0Eh)'s D0 is set 0 at the same time) after the parameter information is sent (= the read function is completed). See also sections: "4.1.3.2.2.2 Acknowledge with Error Report (AwER)" and "5.3.9 Read Display Signal Mode (0Eh)".								
Restriction		None									
Register Availability		<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>								
Default		<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table>								
Flow Chart										

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5.3.4. Read Display Status (09h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
09h	1st	R	D31	0	0	0	0	D26	0	D24	00h
	2nd	R	D23	0	0	0	D19	0	D17	D16	01h
	3rd	R	0	0	0	D12	D11	D10	D9	D8	00h
	4th	R	D7	D6	D5	0	0	0	0	D0	00h

Description

This command indicates the current status of the display, as described in the table below:

Bit	Description	Value	Status
D31	Booster voltage status	0	Booster Off
		1	Booster On
D26	RGB/BGR order	0	RGB (When MADCTL D3 = 0)
		1	BGR (When MADCTL D3= 1)
D24	Source scan sequence	0	Source output Left to Right (When MADCTL D1 = 0)
		1	Source output Right to Left (When MADCTL D1 = 1)
D23	Gate scan sequence	0	Gate output Top to Bottom (When MADCTL D0 = 0)
		1	Gate output Bottom to Top (When MADCTL D0 = 1)
D19	Idle Mode On/Off	0	Idle Mode Off
		1	Idle Mode On
D17	Sleep In/Out	0	Sleep In Mode
		1	Sleep Out Mode
D16	Display Normal Mode On/Off	0	Display Normal Mode Off (All Pixels Off or All Pixels On mode)
		1	Display Normal Mode On
D13	Inversion status	0	Inversion Off
		1	Inversion On
D12	All Pixel On	0	Normal mode
		1	All Pixels On
D11	All Pixel Off	0	Normal mode
		1	All Pixels Off
D10	Display ON/OFF	0	Display is OFF
		1	Display is ON
D9	TE ON/OFF	0	TE OFF
		1	TE ON
D8	Gamma Curve Selection [2:0]	000	Gamma Curve 1
D7		others	Not defined
D6			
D5	TE Mode	0	TE Mode 1
		1	TE Mode 2
D0	Parity Error on DSI	0	No Parity Error
		1	Parity Error

Restriction	None

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Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	00h_01h_00h_00h
S/W Reset	00h_01h_00h_00h
H/W Reset	00h_01h_00h_00h

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5.3.5. Read Display Power Mode (0Ah)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
0Ah	1st	R	D7	D6	0	D4	D3	D2	0	0	08h

Description

0A: RDDPM (Read Display Power Mode).

This command indicates the current status of the display, as described in the table below.

Bit	Description	Value	Status
D7	Booster Voltage Status	0	Booster Off or has a fault.
		1	Booster On and working OK
D6	Idle Mode On/Off	0	Idle Mode Off
		1	Idle Mode On
D4	Sleep In/Out	0	Sleep In Mode
		1	Sleep Out Mode
D3	Display Normal Mode On/Off	0	Display Normal Mode Off
		1	Display Normal Mode On
D2	Display On/Off	0	Display is Off
		1	Display is On

Restriction

None

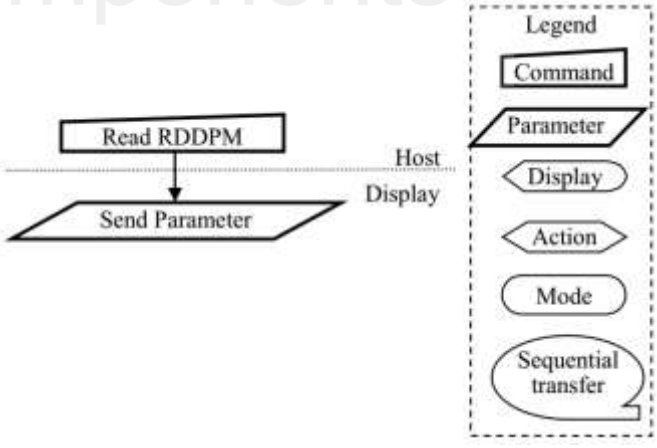
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08h
S/W Reset	08h
H/W Reset	08h

Flow Chart



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5.3.6. Read Display MADCTL (0Bh)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
0Bh	1st	R	0	0	0	0	D3	0	D1	D0	00h

Description

0B: RDDMADCTL (Read Display MADCTL).

This command indicates the current status of the display, as described in the table below.

Bit	Description	Value	Status
D3	RGB/BGR Order (RGB)	0	RGB (When MADCTL D3='0')
		1	BGR (When MADCTL D3='1')
D1	Source scan sequence (SS)	0	Source output Left to Right (When MADCTL D1 = '0')
		1	Source output Right to Left (When MADCTL D1 = '1')
D0	Gate scan sequence (GS)	0	Gate output Top to Bottom (When MADCTL D0 = '0')
		1	Gate output Bottom to Top (When MADCTL D0 = '1')

Note: For Bits D3, D1 and D0 also refer to 5.3.22Memory Access Control (36h).

Restriction

None

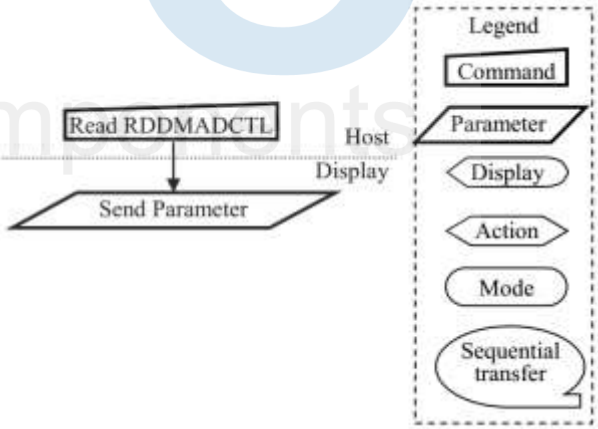
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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5.3.7. Read Display Pixel Format (0Ch)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
0Ch	1st	R	0	0	0	0	0	D[2:0]			07h

Description

0Ch: RDDCOLMOD (Read Display COLMOD).

This command indicates the current status of the display as described in the table below:

DBI[2:0]	Interface Pixel Format
101	16 bit/pixel
110	18 bit/pixel
111	24 bit/pixel
Others	Not defined

Note: For D[2:0] also refer to 5.3.25 Interface Pixel Format (3Ah).

Restriction

None

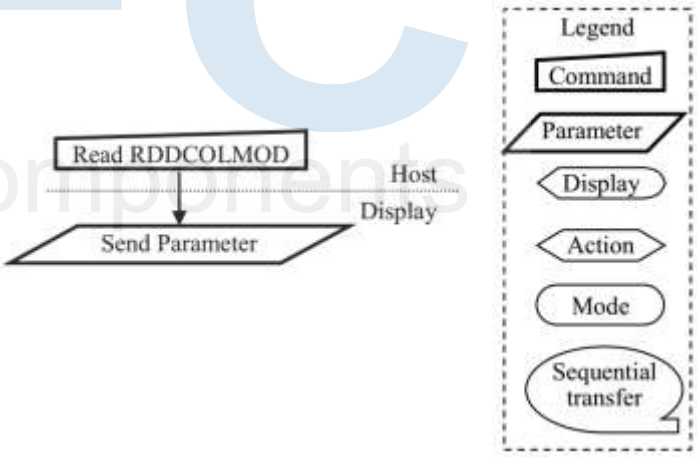
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	07h
S/W Reset	07h
H/W Reset	07h

Flow Chart



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5.3.8. Read Display Image Mode (0Dh)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
0Dh	1st	R	0	0	0	D4	D3	D[2:0]			00h

Description

0D: RDDIM (Read Display Image Mode).

This command indicates the Image Mode status of the display, as described in the Tables below:

Bit	Description	Value	Status
D4	All Pixels On	0	Normal Display
		1	White Display
D3	All Pixels Off	0	Normal Display
		1	Black Display

D[2:0]	Gamma Cure Selection
000	Gamma curve 1
Others	Not defined

Note: For D[2:0] also refer to "5.3.16 Gamma Set (26h)"

Restriction

None

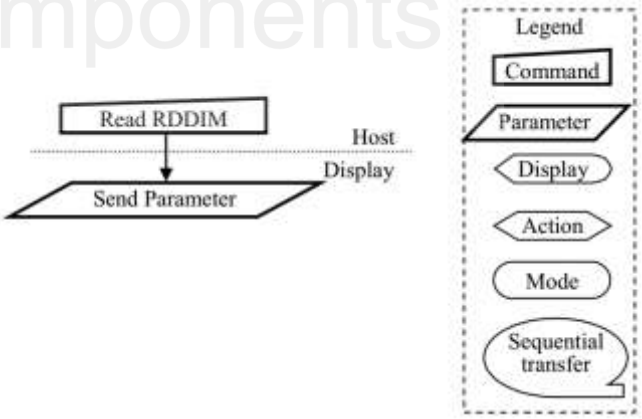
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

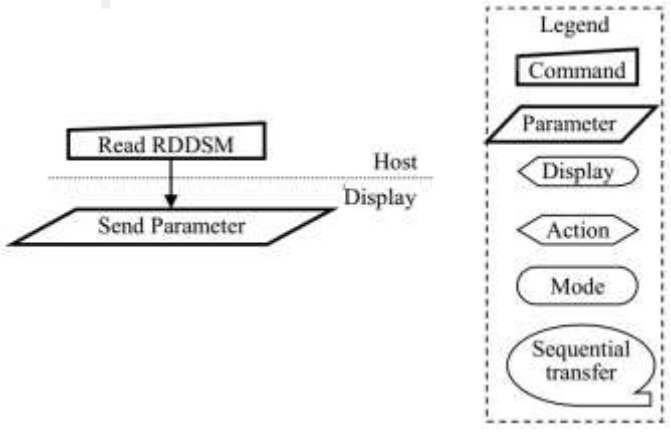
Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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5.3.9. Read Display Signal Mode (0Eh)

<table>
<tr><th colspan="2">Command Page</th><th></th><th colspan="9">Page 0</th></tr>
<tr><th>Address</th><th>Parameter</th><th>W/R</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>0Eh</td><td>1st</td><td>R</td><td>D7</td><td>D6</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>D0</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="11">0E: RDDSM (Read Display Signal Mode).
This command indicates the current status of the display, as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th><th>Status</th></tr>
<tr><td rowspan="2">D7</td><td rowspan="2">Tearing Effect Line On/Off</td><td>0</td><td>Tearing Effect Line Off</td></tr>
<tr><td>1</td><td>Tearing Effect On</td></tr>
<tr><td rowspan="2">D6</td><td rowspan="2">Tearing Effect Line Output Mode</td><td>0</td><td>Tearing Effect Line Mode 1</td></tr>
<tr><td>1</td><td>Tearing Effect Line Mode 2</td></tr>
</table>
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th><th>Status</th></tr>
<tr><td rowspan="2">D0</td><td rowspan="2">Error on DSI</td><td>0</td><td>No Error on DSI</td></tr>
<tr><td>1</td><td>Error on DSI</td></tr>
</table>
See also sections: “4.1.3.2.2.2 Acknowledge with Error Report (AwER)” and “5.3.3 Read Number of the Errors on DSI (05h)”.
Note: For Bit D6, also refer to 5.3.21Tearing Effect Line On (35h).</td></tr>
<tr><td>Restriction</td><td colspan="11">None</td></tr>
<tr><td>Register Availability</td><td colspan="11">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="11">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="11">
</td></tr>
</table>

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5.3.10. Read Display Self-Diagnostic Result (0Fh)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
0Fh	1st	R	D7	D6	0	0	0	0	0	D0	00h

Description

0F: RDDSDR (Read Display Self-Diagnostic Result).

This command indicates the status of the display self-diagnostic results after the Sleep Out command, as described in the table below:

Bit	Description	Action
D7	Register Loading Detection	Invert the D7 bit when the EEPROM and register values are the same.
D6	Functionality Detection	Invert the D6 bit when the chip meets user's functionality requirements.
D0	Checksums Comparison	0 = Checksums are the same 1 = Checksums are not the same

Restriction

It will be necessary to wait 300ms after there is the last write access on Page 0 area registers before there can read Bit D0 value.

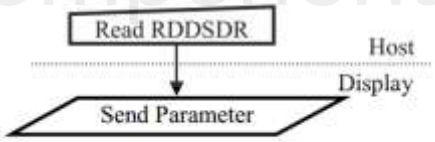
Register Availability

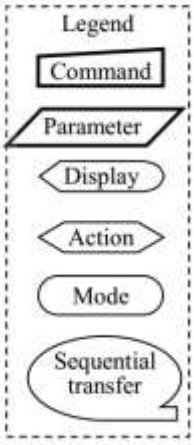
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart





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5.3.11. Sleep In (10h)

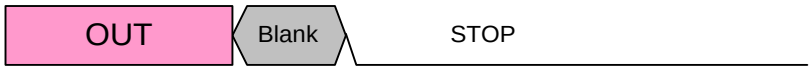
Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
10h	-	W	No Argument								-

Description

10h: SLPIN (Sleep In).

This command causes the ILI9881C-0D to enter the minimum power consumption mode.

In this mode, the DC/DC converter, Internal oscillator, and panel scanning are all stopped.



MCU interface and memory are still working and the memory can keep its contents.

Ambient light based control is off.

Backlights and display are off.

Dimming function does not work when there is changing mode from Sleep Out to Sleep In.

Restriction

This command has no effect when the module is already in the Sleep In mode. To leave the Sleep In Mode, only the Sleep Out Command (11h) is workable. It is necessary to wait 5msec before sending the next command; this is to allow time for the supply voltages and clock circuits to become stable. It is necessary to wait 120msec after sending the Sleep Out command (when in the Sleep In Mode) before the Sleep In command can be sent.

Register Availability

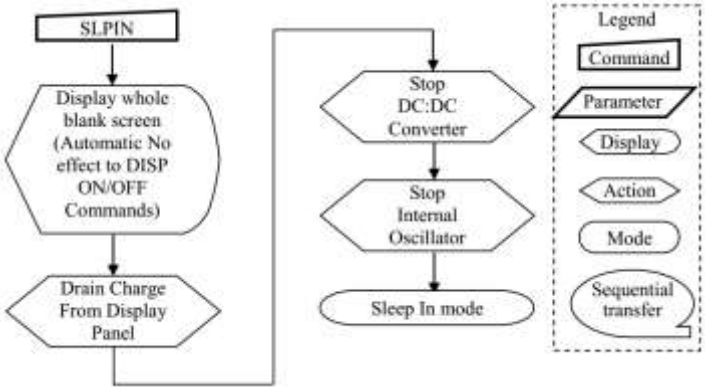
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

Flow Chart

It takes 120msec to get into Sleep In mode after SLPIN command issued.



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5.3.12. Sleep Out (11h)

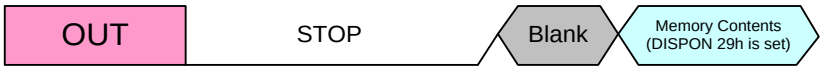
Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
11h	-	W	No Argument								-

Description

11h: SLPOUT (Sleep Out).

This command turns off the sleep mode.

In this mode, the DC/DC converter is enabled, the Internal oscillator is started, and the panel scanning is started.



Restriction

This command has no effect when the module is already in the Sleep Out mode. To leave the Sleep Out mode, only the Sleep In command (10h), SW Reset Command (01h) or HW Reset are workable. It is necessary to wait 5msec before sending the next command; this is to allow time for the supply voltages and clock circuits to become stable.

The Driver IC loads all display supplier's factory default values to the registers during this 5msec. There cannot be any abnormal visual effect on the display image if factory default and register values are the same when this load is done and when the Driver IC is already in the Sleep Out mode. During this 5msec, the Driver IC also performs self-diagnostic functions.

It is necessary to wait 120msec after sending the Sleep In command (when in the Sleep Out mode) before the Sleep Out command can be sent.

Register Availability

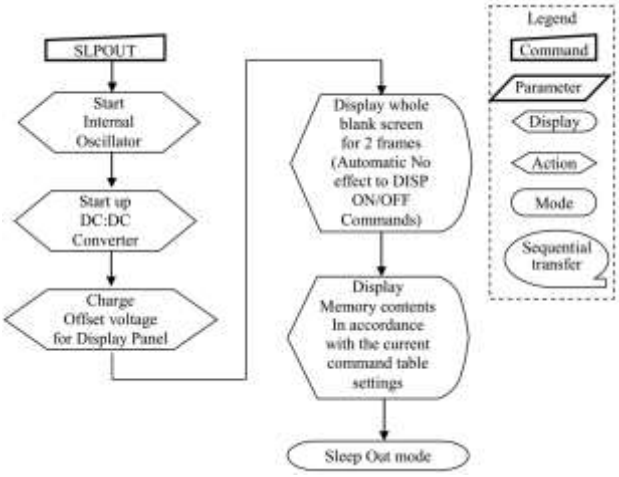
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

Flow Chart

It takes 120msec to become Sleep Out mode after SLPOUT command issued.



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5.3.13. Normal Display Mode On (13h)

<table>
<tr><th colspan="2">Command Page</th><th colspan="10">Page 0</th></tr>
<tr><th>Address</th><th>Parameter</th><th>W/R</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>13h</td><td>-</td><td>W</td><td colspan="9">No Argument</td><td>-</td></tr>
<tr><td colspan="2">Description</td><td colspan="10">13h: NORON (Normal Display Mode On).
This command returns the display to normal mode.</td></tr>
<tr><td colspan="2">Restriction</td><td colspan="10">This command has no effect when the Normal Display Mode is active.</td></tr>
<tr><td colspan="2">Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td colspan="2">Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode On</td></tr><tr><td>S/W Reset</td><td>Normal Display Mode On</td></tr><tr><td>H/W Reset</td><td>Normal Display Mode On</td></tr></table></td></tr>
<tr><td colspan="2">Flow Chart</td><td colspan="10"></td></tr>
</table>

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5.3.14. All Pixel Off (22h)

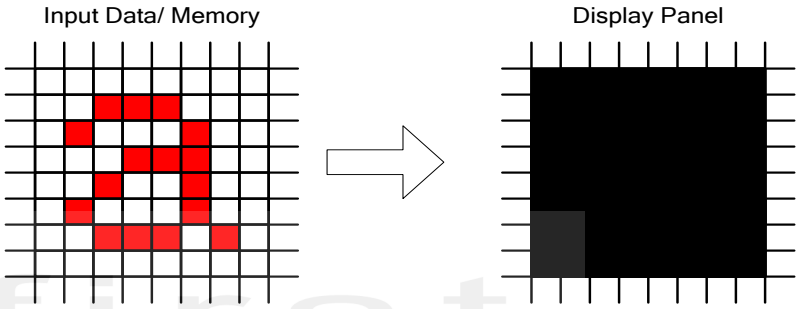
Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
22h	-	W	No Argument								-

Description

22h: ALLPOFF (All Pixels Off).

This command turns the display panel black in 'Sleep Out' mode and a status bit of the 'Read Display Image Mode' register (0Dh) can be read.

This command makes no change of contents of the input data (or frame memory). This command does not change any other status.



'All Pixels On' or 'Normal Display Mode On' commands are used to leave this mode. When ILI9881C-0D works in 'Idle Mode On' and 'Sleep Out' state, the display panel is showing the content of the frame memory after 'Normal Display Mode On' commands.

Restriction

This command has no effect when module is already in all pixels off mode.

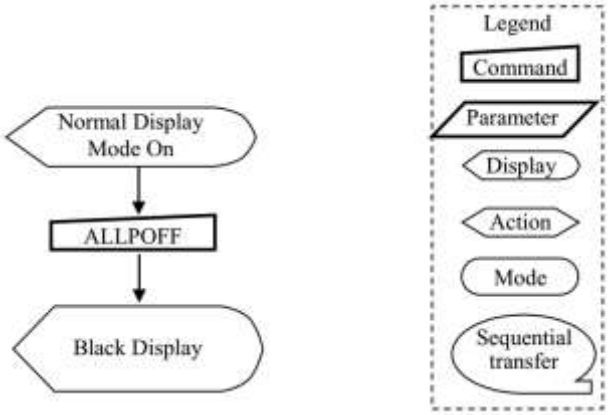
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
S/W Reset	OFF
H/W Reset	OFF

Flow Chart



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5.3.15. All Pixel On (23h)

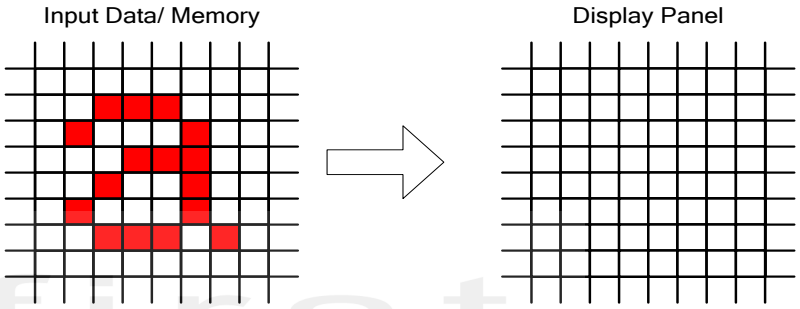
Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
23h	-	W	No Argument								-

Description

23h: ALLPON (All Pixels On).

This command turns the display panel white in 'Sleep out' mode and a status bit of the 'Read Display Image Mode' register (0Dh) can be read.

This command makes no change of contents of the input data (or frame memory). This command does not change any other status.



'All Pixels Off' or 'Normal Display Mode On' commands are used to leave this mode.

When ILI9881C-0D works in 'Idle Mode On' and 'Sleep Out' state, the display panel is showing the content of the frame memory after 'Normal Display Mode On' commands.

Restriction

This command has no effect when module is already in all pixels on mode.

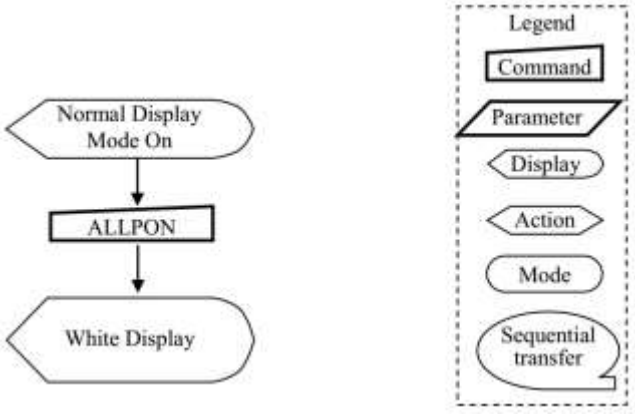
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
S/W Reset	OFF
H/W Reset	OFF

Flow Chart



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5.3.16. Gamma Set (26h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
26h	1st	W	0	0	0	0	GC [3:0]				01h

Description

26h: GAMSET (Gamma Set).

This command is used to select the desired Gamma curve for the current display. A maximum of 1 fixed Gamma curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table below:

GC [3:0]	Curve Selected
1h	Gamma curve 1
Other	Reserved

Note: All others value are undefined.

Restriction

Values of GC [3:0] not shown in the table above are invalid and will not change the current selected Gamma curve until a valid value is received.

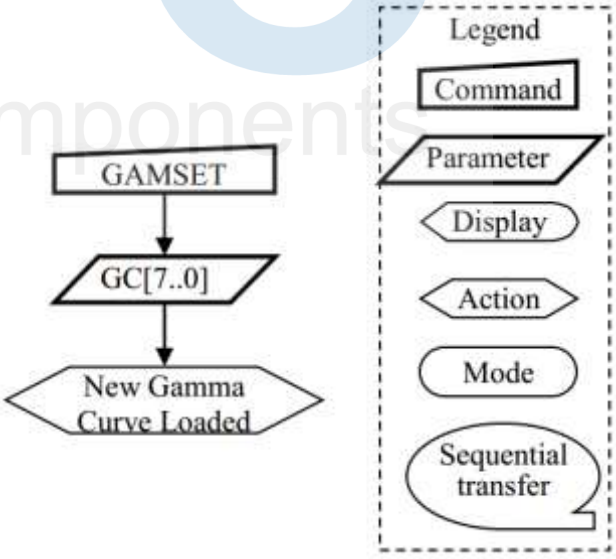
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

Flow Chart



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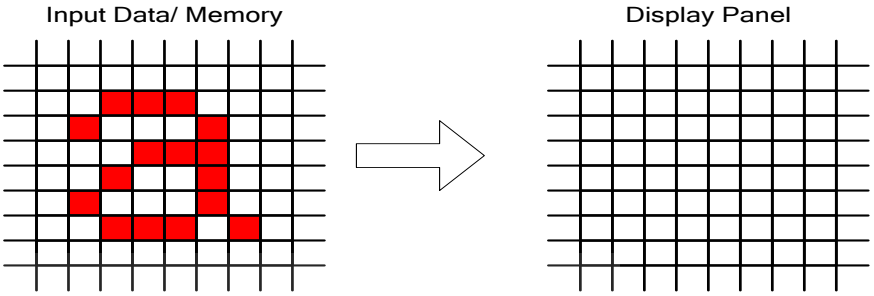
5.3.17. Display Off (28h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
28h	-	W	No Argument								-

Description

28h: DISPOFF (Display Off)

This command is used to enter into the Display Off mode. Output from the input data (or frame memory) is disabled and a blank page inserted. This command makes no change of contents of the input data (or frame memory) and does not change any other status. There will be no abnormal visible effect on the display.



Restriction

This command has no effect when the module is already in the Display Off mode.

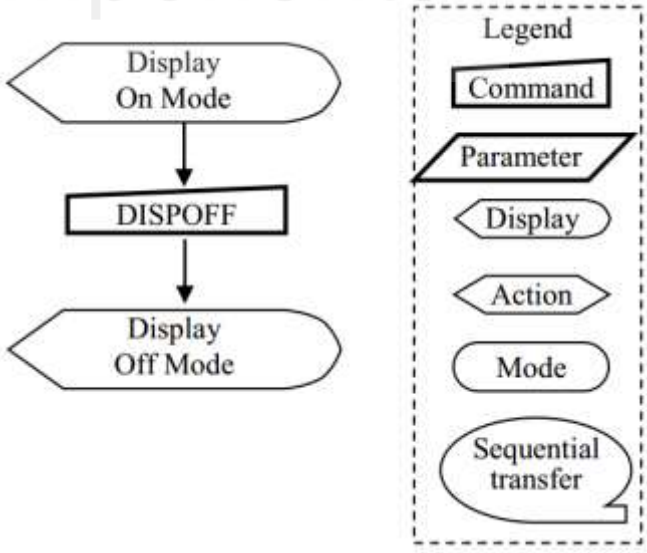
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



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5.3.18. Display ON (29h)

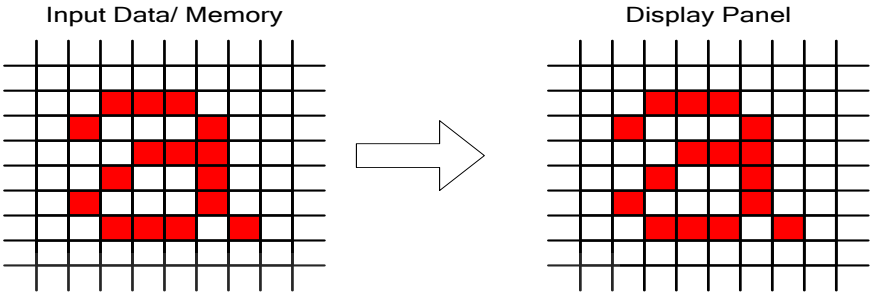
Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
29h	-	W	No Argument								-

Description

29h: DISPON (Display On).

This command is used to recover from the Display Off mode. Output from the input data (or frame memory) is enabled.

This command makes no change of contents of the input data (or frame memory) and does not change any other status.



Restriction

This command has no effect when the ILI9881C-0D is already in the Display On mode.

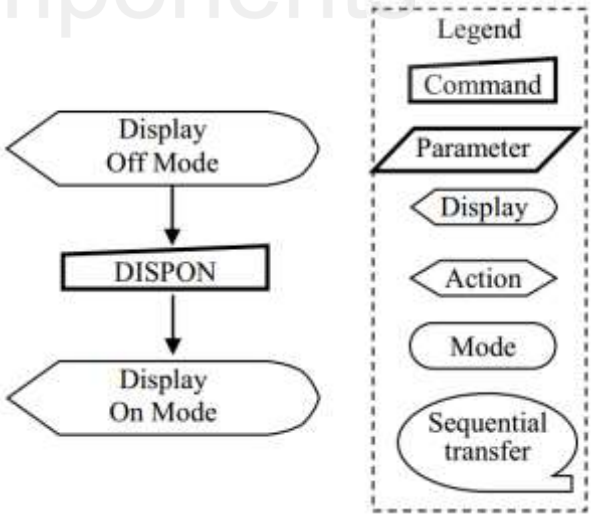
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



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5.3.19. Memory Write (2Ch)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
2Ch	1st	W	D1[23:16]								00~FFh
	2nd	W	D1[15:8]								00~FFh
	3rd	W	D1[7:0]								00~FFh
	…	W	…								00~FFh
	Nth	W	Dn[7:0]								00~FFh

Description

2Ch: RAMWR (Memory Write).

This command transfers data from the MCU to the Frame Memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to zero.

Then D[23:0] is stored in the Frame Memory and the column register and the page register incremented at the same time. Sending any other command can stop frame Write.

Restriction

This command's parameter length must be based on 2 pixel data length (6 bytes) (N=3 x n, N is multiple of 6).

When ILI9881C-0D's work state is "Normal Mode On, Idle Mode On and Sleep Out", full-resolution frame data must be send by Memory Write (2Ch) and Memory Write Continue (3Ch) command.

Transmission sequences: LP_00 → HS for R2Ch → LP_00 → HS for R3Ch → LP_00 → HS for CMD → LP_00

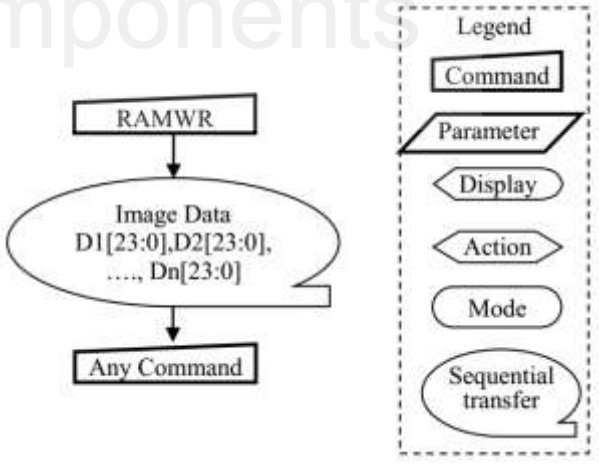
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is set randomly
H/W Reset	Contents of memory is set randomly

Flow Chart



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5.3.20. Tearing Effect Line Off (34h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
34h	-	W	No Argument								-
Description	34h: TEOFF (Tearing Effect Line OFF). This command is used to turn off the Display module's Tearing Effect output signal from the TE signal line.										
Restriction	This command has no effect when the Tearing Effect output is already off.										

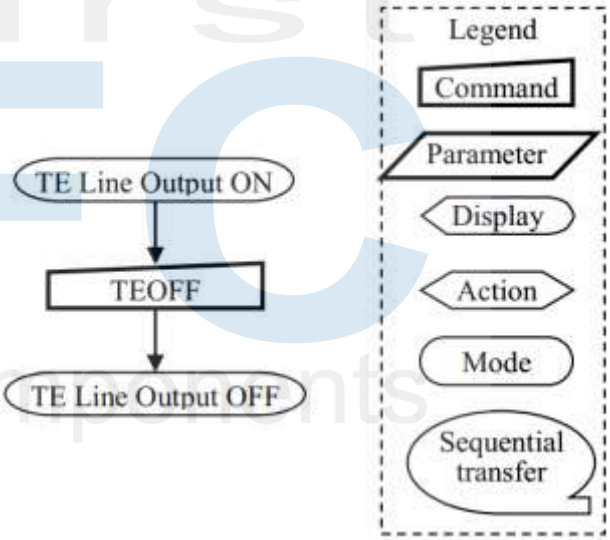
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart



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5.3.21. Tearing Effect Line On (35h)

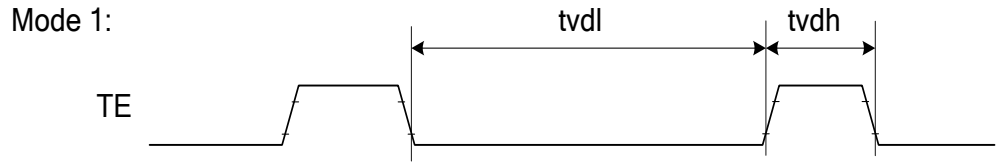
Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
35h	1st	W	0	0	0	0	0	0	0	M	00

Description

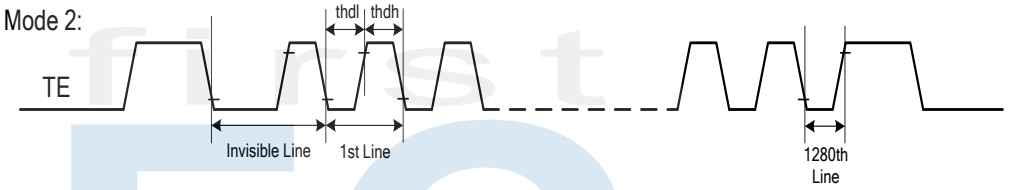
35h: TEON (Tearing Effect Line ON).

This command is used to turn on the Tearing Effect output signal from the TE signal line. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

When **M=0**: The Tearing Effect Output line consists of V-Blanking information only:



When **M=1**: The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:



Note : The Tearing Effect Output line shall be low when the display module is in Sleep mode

Restriction

This command has no effect when the Tearing Effect output is already ON.

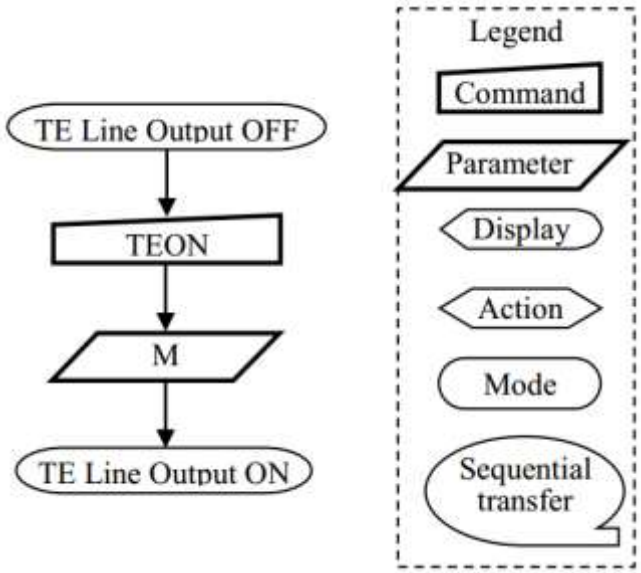
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

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Flow Chart	

first FC components

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5.3.22. Memory Access Control (36h)

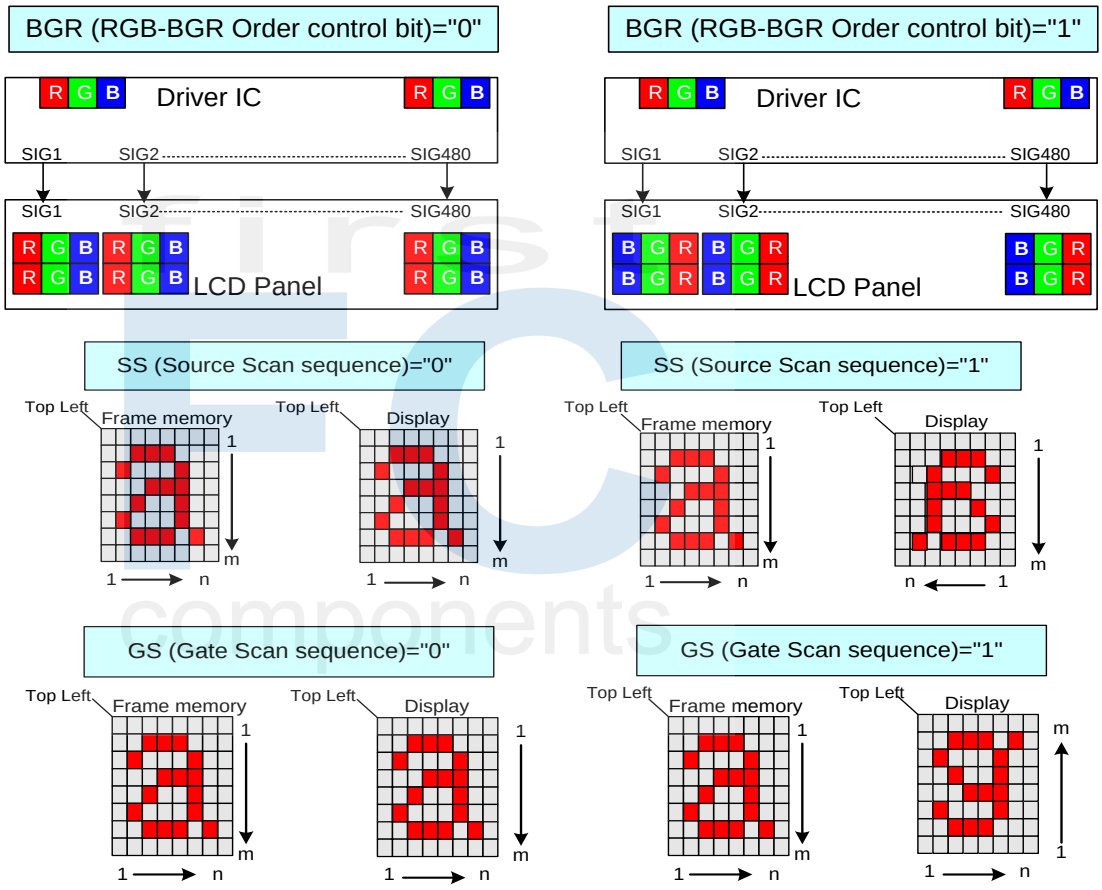
Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
36h	1st	W	0	0	0	0	BGR	0	SS	GS	00h

Description

36h: MADCTL (Memory Access Control).

This command makes no change on the other status of the driver.

Bit	Symbol	Name	Description
D3	BGR	RGB/BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
D1	SS	Flip Horizontal (SS)	Select the Source driver scan direction on the panel module
D0	GS	Flip Vertical (GS)	Select the Gate driver scan direction on the panel module



Restriction: None

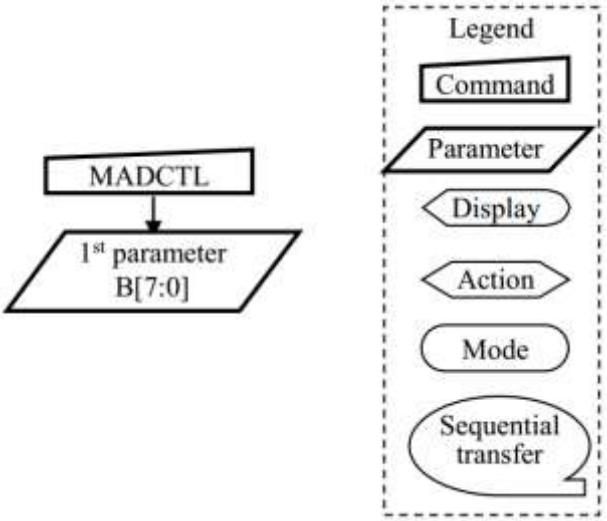
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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Flow Chart	

first FC components

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5.3.23. Idle Mode Off (38h)

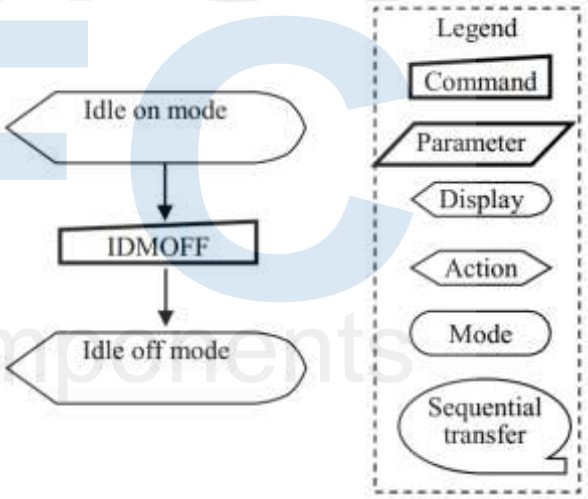
Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
38h	-	W	No Argument								-
Description	38h: IDMOFF (Idle mode off). This command causes the Display module to exit the Idle mode. In the Idle Mode Off, the display panel can display a maximum of 16.7M colors.										
Restriction	This command has no effect when the module is already in the Idle Mode Off.										
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

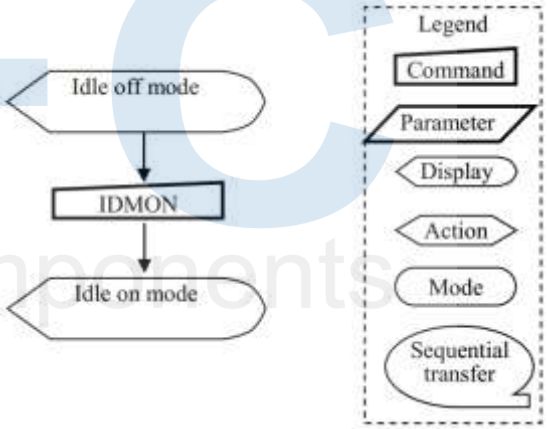
Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart



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5.3.24. Idle Mode On (39h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
39h	-	W	No Argument								-
Description	39h: IDMON (Idle mode on). This command is used to enter into the Idle Mode On. In the Idle Mode On, color expression is reduced. The display panel shows de-compressed content of frame memory in the Idle Mode On and Sleep Out states. The primary color of “Normal Black” panel is black, the secondary color is defined by “Write Idle Mode Color” (80h) command.										
Restriction	This command has no effect when the module is already in the Idle Mode On.										
Register Availability	Status / Availability: Normal Mode On, Idle Mode Off, Sleep Out — Yes Normal Mode On, Idle Mode On, Sleep Out — Yes Sleep In — Yes										
Default	Status / Default Value: Power On Sequence — Idle Mode Off S/W Reset — Idle Mode Off H/W Reset — Idle Mode Off										
Flow Chart											

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5.3.25. Interface Pixel Format (3Ah)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
3Ah	1st	W	0	0	0	0	0	DBI[2:0]			07h

Description

3A: COLMOD (Interface Pixel Format).

This command is used to define the format of RGB picture data, which is to be transferred via the MIPI DSI Command Mode. The formats are shown in the table:

Interface Format	DBI[2:0]
Not Defined	000
Not Defined	001
Not Defined	010
Not Defined	011
Not Defined	100
16 bit/pixel	101
18 bit/pixel	110
24 bit/pixel	111

Restriction

There is no visible effect until the Frame Memory is written to.

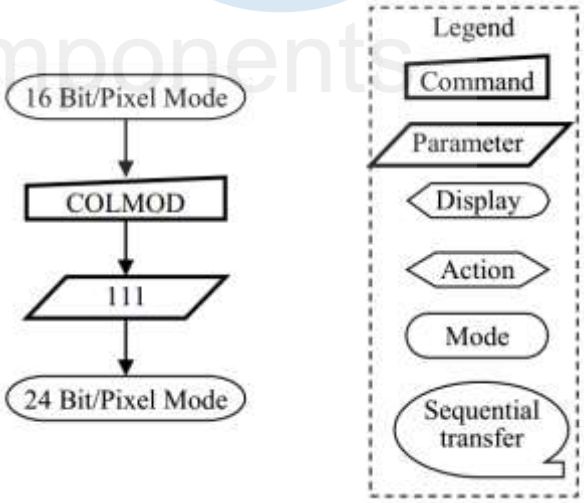
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	07h
S/W Reset	07h
H/W Reset	07h

Flow Chart



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5.3.26. Memory Write Continue (3Ch)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
3Ch	1st	W	D1[23:16]								00~FFh
	2nd	W	D1[15:8]								00~FFh
	3rd	W	D1[7:0]								00~FFh
	…	W	…								00~FFh
	Nth	W	Dn[7:0]								00~FFh

Description

3Ch: RAMWRC (Memory Write Continue).

This command is used to transfer data from the MCU to the Frame Memory, if want to continue the Frame Memory write after the "Memory Write (2Ch)" command. This command makes no change to the status of the other driver. When this command is accepted, the column register and the page register are not reset to zero since it has been done on "Memory Write (2Ch)" command.

Sending any other command can stop frame Write.

Restriction

This command's parameter length must be based on 2 pixel data length (6 bytes) (N=3 x n, N is multiple of 6).

Transmission sequences: LP_00 → HS for R2Ch → LP_00 → HS for R3Ch → LP_00 → HS for CMD → LP_00

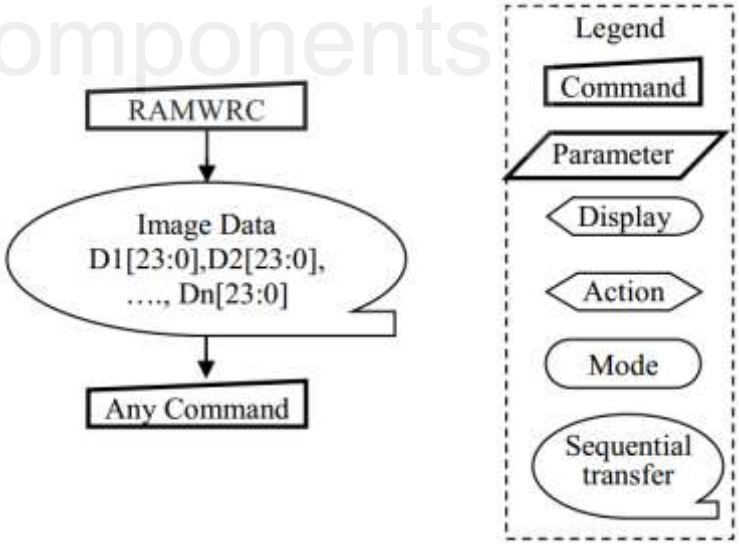
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is set randomly
H/W Reset	Contents of memory is set randomly

Flow Chart



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5.3.27. Set_Tear_Scanline (44h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
44h	1st	W	0	0	0	0	0	TE_LINE[10:8]			00h
	2nd	W	TE_LINE[7:0]								00h

Description

44h: SET_TEAR_SCANLINE.

This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N.

The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode. After issuing a set_tear_scanline command to the display module, the Tearing Effect output signal, e.g. as in DBI-2 systems, shall be a delayed version of V-Blanking information as illustrated by below figure.

In other words, the TE pulse width needs to be identical with normal mode Vsync related TE pulse.



Note that set_tear_scanline with N = 0 is equivalent to set_tear_on with M = 0.

The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

Restriction

This command takes affect on the frame following the current frame.

Therefore, if the Tear Effect (TE) output is already ON, the TE output shall continue to operate as programmed by the previous set_tear_on, or set_tear_scanline, command until the end of the frame.

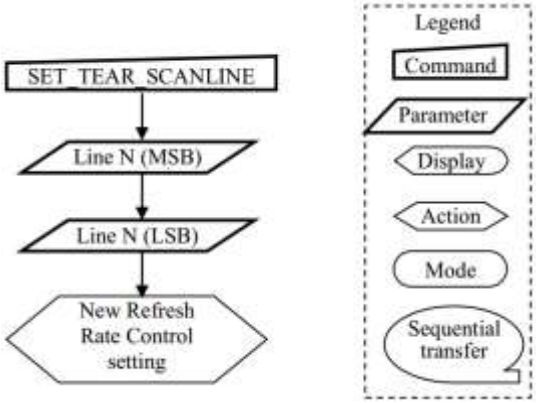
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	No

Default

Status	Default Value
Power On Sequence	N=0
S/W Reset	N=0
H/W Reset	N=0

Flow Chart



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5.3.28. Get_Tear_Scanline (45h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
45h	1st	R	0	0	0	0	0	TE_LINE[10:8]			00h
	2nd	R	TE_LINE[7:0]								00h
Description			45h: GET_TEAR_SCANLINE. This command returns setting value of Set_Tear_Scanline command (44h).								
Restriction			None								

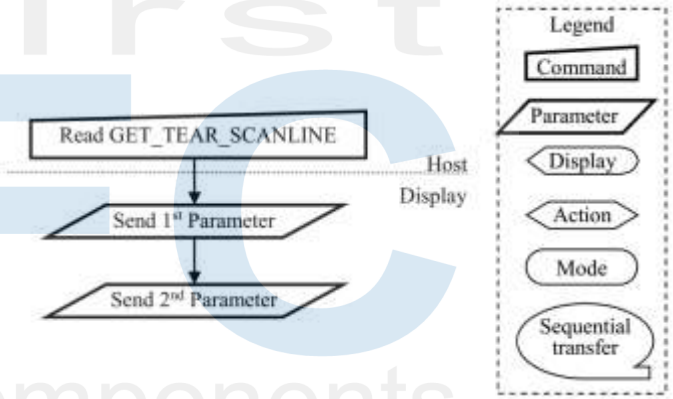
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	No

Default

Status	Default Value
Power On Sequence	N=0
S/W Reset	N=0
H/W Reset	N=0

Flow Chart



first components

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5.3.29. Write Display Brightness Value (51h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
51h	1st	W	0	0	0	0	DBV[11:8]				00h
	2nd	W	DBV[7:0]								00h
Description			51h: WRDISBV (Write Display Brightness). This command is used to adjust the brightness value of the display. DBV[11:0]: 12 bit, for display brightness of manual brightness setting and the CABC in the ILI9881C-0D. PWM output signal and LEDPWM pin will control the LED driver IC in order to control the display brightness. In principle relationship is that 0000h value means the lowest brightness and 0FFFh value means the highest brightness.								
Restriction			None								

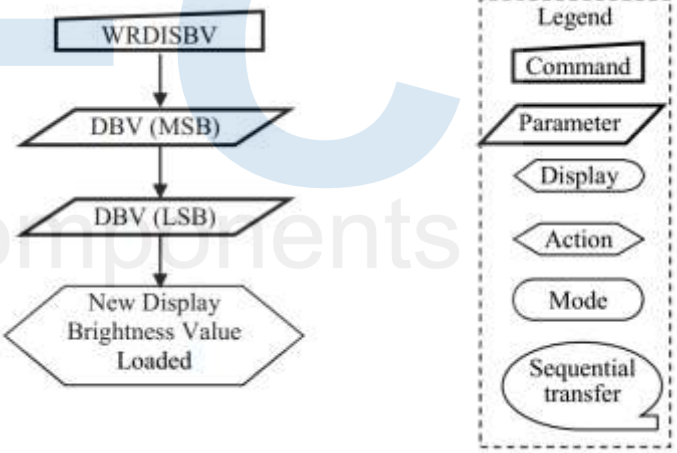
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h
S/W Reset	00h_00h
H/W Reset	00h_00h

Flow Chart



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5.3.30. Read Display Brightness Value (52h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
52h	1st	R	0	0	0	0	DBV[11:8]				00h
	2nd	R	DBV[7:0]								00h

Description

52h: RDDISBV (Read Display Brightness Value).

This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification.

In principle the relationship is that 0000h value means the lowest brightness and 0FFFh value means the highest brightness.

DBV[11:0] is reset when display is in sleep-in mode.

DBV[11:0] is '0' when bit BCTRL of "5.3.31Write CTRL Display Value (53h)" command is '0'.

DBV[11:0] is manual set brightness specified with "5.3.31Write CTRL Display Value (53h)" command when bit BCTRL is '1'.

Restriction

None

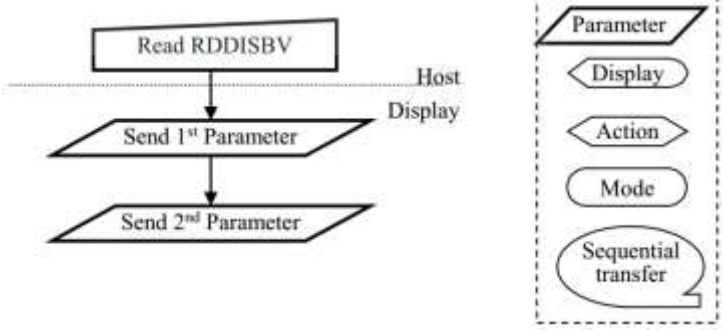
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h
S/W Reset	00h_00h
H/W Reset	00h_00h

Flow Chart



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5.3.31. Write CTRL Display Value (53h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
53h	1st	W	0	0	BCTRL	0	DD	BL	0	0	00h

Description

53h: WRCTRLD (Write Control Display).

This command is used to control the display brightness.

BCTRL: Brightness Control Block On/Off. This bit is always used to switch brightness for display.

BCTRL	Description
0	Brightness Control Block Off (DBV[11:0] = 0000h)
1	Brightness Control Block On (DBV[11:0] is active)

DD: Display Dimming Control.

DD	Description
0	Display Dimming Off
1	Display Dimming On

BL: Backlight Control On/Off

BL	Description
0	Backlight Control Off
1	Backlight Control On

Dimming function is adapted to the brightness registers for display when the bit BCTRL is changed at DD = 1, e.g. BCTRL: 0-> 1 or 1-> 0.

When the BL bit changes from 'ON' to 'OFF', backlight is turned off without gradual dimming, even if Display Dimming On (DD = 1) are selected.

Restriction

None

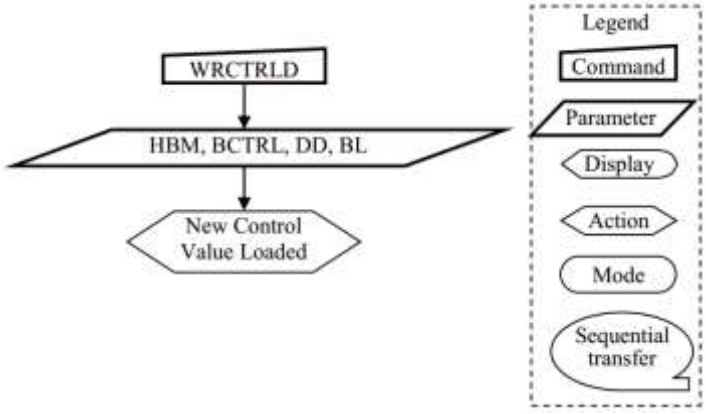
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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5.3.32. Read CTRL Display Value (54h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
54h	1st	R	0	0	BCTRL	0	DD	BL	0	0	00h

Description

54h: RDCTRLD (Read Control Value Display).

This command returns the display brightness control values.

BCTRL: Brightness Control Block On/Off. This bit is always used to switch brightness for display.

BCTRL	Description
0	Brightness Control Block Off (DBV[11:0] = 0000h)
1	Brightness Control Block On (DBV[11:0] is active)

DD: Display Dimming Control.

DD	Description
0	Display Dimming Off
1	Display Dimming On

BL: Backlight Control On/Off

BL	Description
0	Backlight Control Off
1	Backlight Control On

Dimming function is adapted to the brightness registers for display when the bit BCTRL is changed at DD = 1, e.g. BCTRL: 0-> 1 or 1-> 0.

When the BL bit changes from 'ON' to 'OFF', backlight is turned off without gradual dimming, even if Display Dimming On (DD = 1) are selected.

Restriction

None

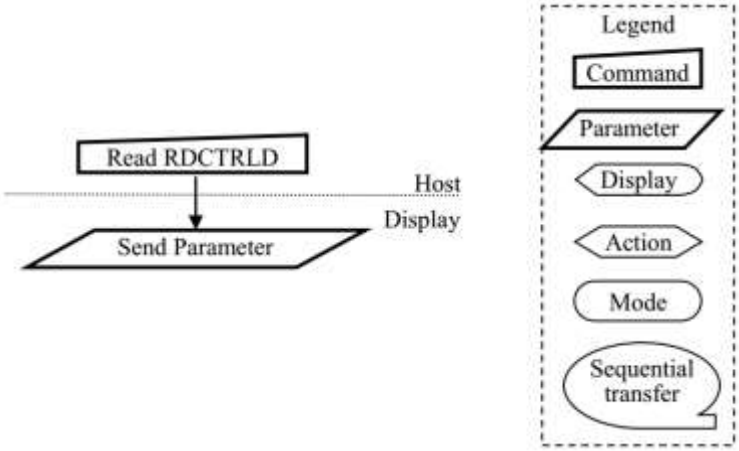
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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5.3.33. Write Power Save (55h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
55h	1st	W	PWRSAVE[7:0]								00h

Description

55h: PWRSAVE (Write Power Save).

This command is used to write the settings for power save control functionalities.

PWRSAVE[7:0]	Function	Note
00000000	Power Save Off	-
00000001	Power Save Low	Conservative Setting of CABC/DBLC
00000010	Power Save Medium	Medium Setting of CABC/DBLC
00000011	Power Save High	Aggressive Setting of CABC/DBLC
1000XXXX	IE On – Low	Low Enhancement of LCD
1001XXXX	IE On – Medium	Medium Enhancement of LCD
1011XXXX	IE On – High	High Enhancement of LCD
0100XXXX	SRE - Low	Sunlight readability enhancement
0101XXXX	SRE - Medium	Sunlight readability enhancement
0110XXXX	SRE - High	Sunlight readability enhancement
Others	Reserved	-

CABC = Content Adaptive Brightness Control

DBLC = Dynamic Backlight Control

IE = Image Enhancement

Restriction

None

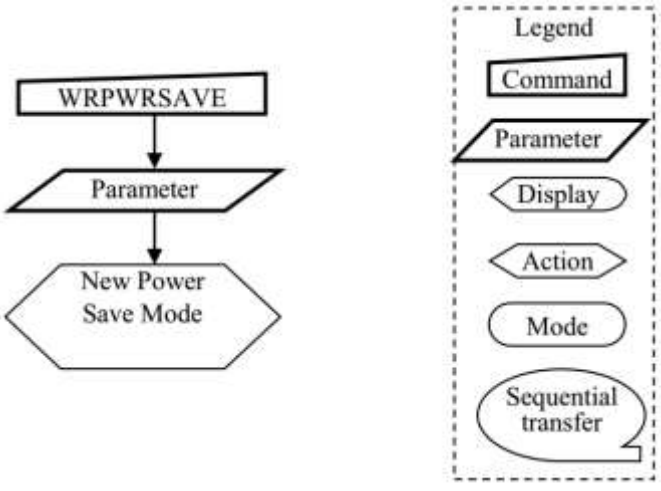
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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5.3.34. Read Power Save (56h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
56h	1st	R	PWRSAVE[7:0]								00h

Description

56h: RDPWRSAVE (Read Power Save).

This command is used to read the settings for power save control functionalities.

PWRSAVE[7:0]	Function	Note
00000000	Power Save Off	-
00000001	Power Save Low	Conservative Setting of CABC/DBLC
00000010	Power Save Medium	Medium Setting of CABC/DBLC
00000011	Power Save High	Aggressive Setting of CABC/DBLC
1000XXXX	IE On – Low	Low Enhancement of LCD
1001XXXX	IE On – Medium	Medium Enhancement of LCD
1011XXXX	IE On – High	High Enhancement of LCD
0100XXXX	SRE - Low	Sunlight readability enhancement
0101XXXX	SRE - Medium	Sunlight readability enhancement
0110XXXX	SRE - High	Sunlight readability enhancement
Others	Reserved	-

CABC = Content Adaptive Brightness Control

DBLC = Dynamic Backlight Control

IE = Image Enhancement

Restriction

None

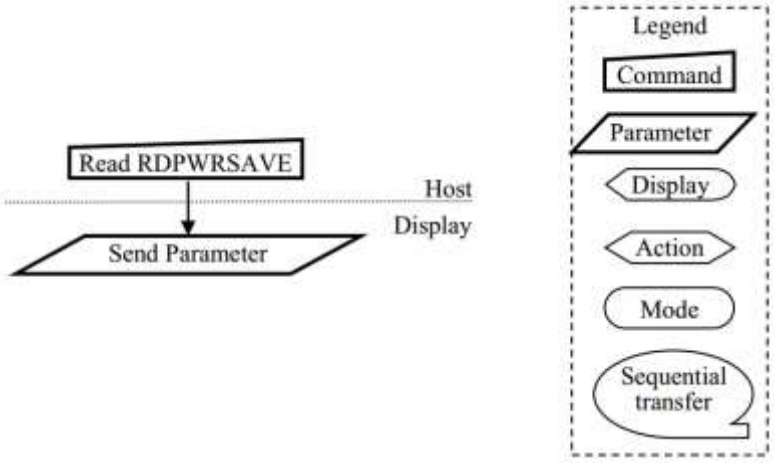
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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5.3.35. Stop Transition (59h)

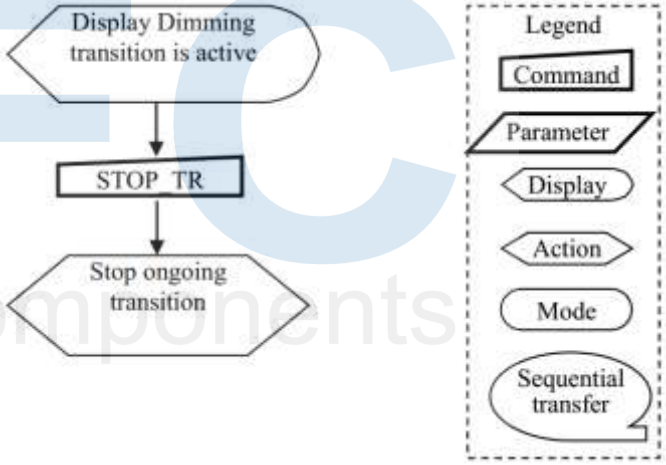
Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
59h	-	W	No Argument								-
Description	59h: STOP_TR (Stop Transition). When DD bit status of "5.3.31Write CTRL Display Value (53h)" register is '1', applying this command instantly stops the ongoing transition of Display Dimming. When display module receives this command, the current output value stays active.										
Restriction	This command has no effect when Display Dimming transition is not active.										
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart



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5.3.36. Write CABC Minimum Brightness (5Eh)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
5Eh	1st	W	0	0	0	0	CMB[11:8]				00h
	2nd	W	CMB[7:0]								00h
Description	5Eh: WRCABCMB (Write CABC minimum brightness). This command is used to set the minimum brightness value of the display for CABC function. In principle relationship is that 0000h value means the lowest brightness for CABC and 0FFFh value means the highest brightness for CABC.										
Restriction	None										

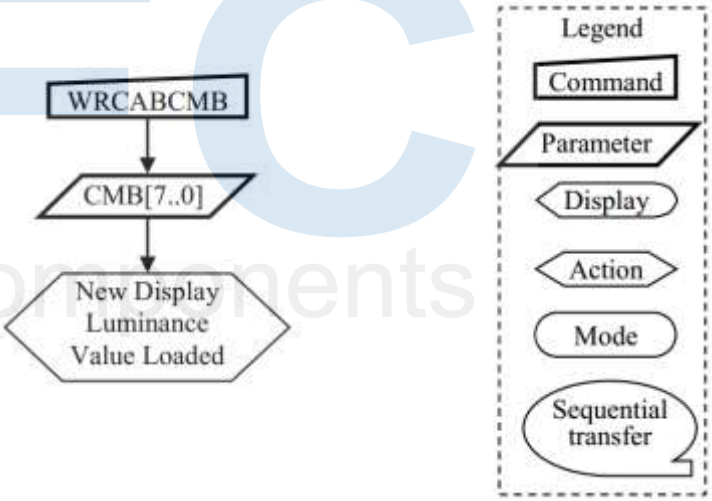
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h
S/W Reset	00h_00h
H/W Reset	00h_00h

Flow Chart



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5.3.37. Read CABC Minimum Brightness (5Fh)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
5Fh	1st	R	0	0	0	0	CMB[11:8]				00h
	2nd	R	CMB[7:0]								00h
Description	5Fh: RDCABCMB (Read CABC Minimum Brightness). This command returns the minimum brightness value of CABC function. In principle the relationship is that 0000h value means the lowest brightness and 0FFFh value means the highest brightness. CMB[11:0] is CABC minimum brightness specified by the Write CABC minimum brightness (5Eh) command.										
Restriction	None										

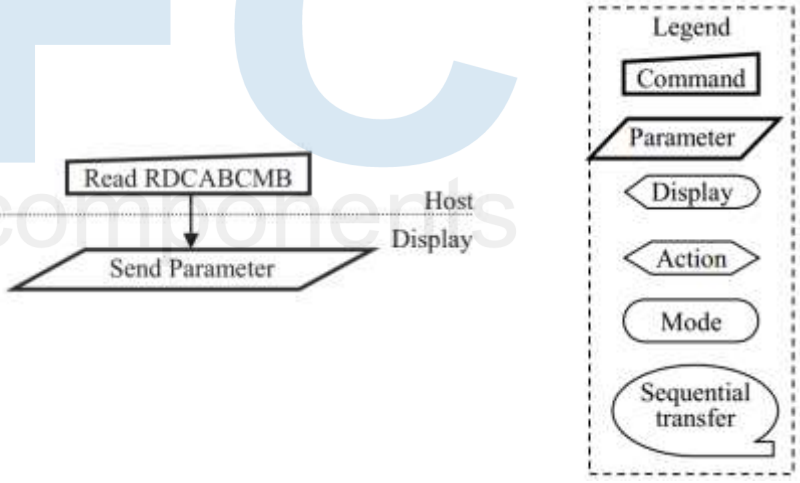
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h
S/W Reset	00h_00h
H/W Reset	00h_00h

Flow Chart



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5.3.38. Set Transition Time (68h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
68h	1st	W	TT_STP[7:0]								00h
	2nd	W	ST_TIM[7:0]								00h

Description

68h: SET_TT (Set Transition Time).

This command controls the total transition time of Display Dimming function.

Transition time is adjusted with two parameters, defining as follows:

1st Parameter TT_STP [7:0] defines the number of dimming steps for transition.

TT_STP [7:0]	Description
00h	1 step
01h	2 step
02h	4 step
03h	8 step
04h	16 step
05h	32 step
06h	64 step
07h	128 step
08h	256 step
09h	512 step
0Ah	1024 step
0Bh	2048 step
0Ch	4096 step
Others	Reserved

2nd Parameter ST_TIM [7:0] defines the step time as frame units for each dimming step.

ST_TIM [7:0]	Description
00h	1 frame
01h	1 frame
02h	2 frame
03h	3 frame
04h	4 frame
05h	5 frame
:	:
:	:
FBh	251 frame
FCh	252 frame
FDh	253 frame
FEh	254 frame
FFh	255 frame

Thereby, total transition time for dimming can be calculated as follows:

TT_STP [7:0] * ST_TIM [7:0] = TT, where TT unit is frame. Value 0000h means the transition is instant

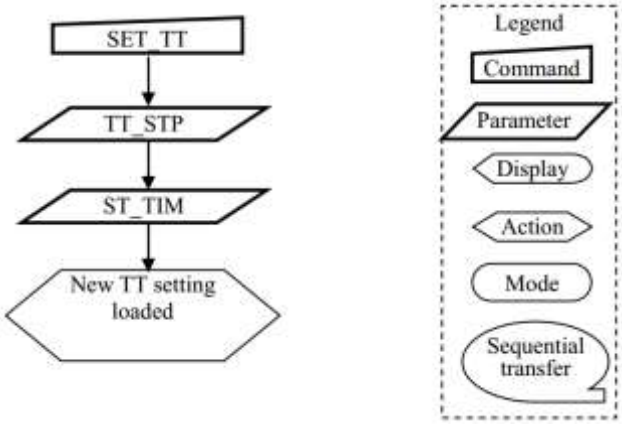
Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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<table>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h_00h</td></tr>
<tr><td>S/W Reset</td><td>00h_00h</td></tr>
<tr><td>H/W Reset</td><td>00h_00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>
</td></tr>
</table>

first FC components

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5.3.39. Get Transition Time (69h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
69h	1st	R	TT_STP[7:0]								00h
	2nd	R	ST_TIM[7:0]								00h

Description

69h: GET_TT (Get Transition Time Value).

This readout returns the Transition Time value of Display Dimming function, described in section “5.3.38Set Transition Time (68h)”.

Transition time is adjusted with two parameters, defining as follows:

1st Parameter TT_STP [7:0] defines the number of dimming steps for transition.

TT_STP [7:0]	Description
00h	1 step
01h	2 step
02h	4 step
03h	8 step
04h	16 step
05h	32 step
06h	64 step
07h	128 step
08h	256 step
09h	512 step
0Ah	1024 step
0Bh	2048 step
0Ch	4096 step
Others	Reserved

2nd Parameter ST_TIM [7:0] defines the step time as frame units for each dimming step.

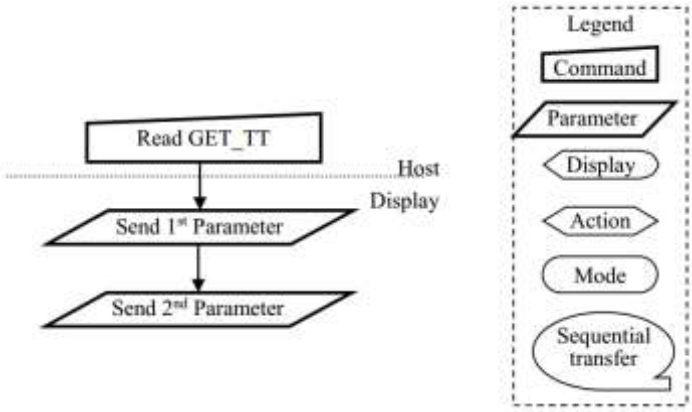
ST_TIM [7:0]	Description
00h	1 frame
01h	1 frame
02h	2 frame
03h	3 frame
04h	4 frame
05h	5 frame
:	:
:	:
FBh	251 frame
FCh	252 frame
FDh	253 frame
FEh	254 frame
FFh	255 frame

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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<table>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h_00h</td></tr>
<tr><td>S/W Reset</td><td>00h_00h</td></tr>
<tr><td>H/W Reset</td><td>00h_00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>
</td></tr>
</table>

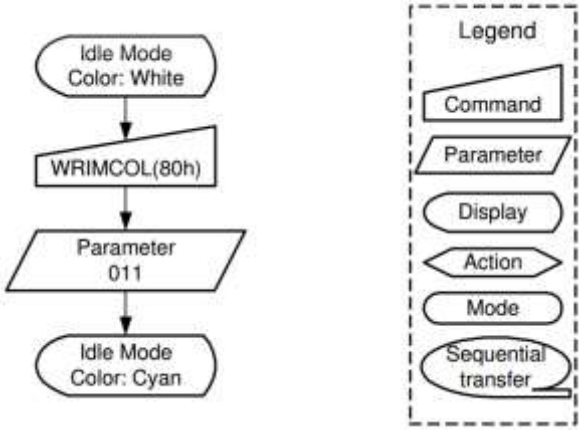
first FC components

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5.3.40. Write Idle Mode Color (80h)

<table>
<tr><th colspan="2">Command Page</th><th></th><th colspan="9">Page 0</th></tr>
<tr><th>Address</th><th>Parameter</th><th>W/R</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>80h</td><td>1st</td><td>W</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>R</td><td>G</td><td>B</td><td>07h</td></tr>
<tr><td>Description</td><td colspan="11">80h: WRIMCOL.
This command can be used to select color for Idle Mode.
Color selection is defined in the following table:

<table>
<tr><th>Idle Mode Color Selection</th><th>R</th><th>G</th><th>B</th></tr>
<tr><td>Black</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Blue</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Green</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Cyan</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Red</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Magenta</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>Yellow</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>White</td><td>1</td><td>1</td><td>1</td></tr>
</table>

Default setting for color selection for “Normal Black” panel is ‘White’; R=G=B:’1’.</td></tr>
<tr><td>Restriction</td><td colspan="11">None</td></tr>
<tr><td>Register Availability</td><td colspan="11">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="11">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>07h</td></tr>
<tr><td>S/W Reset</td><td>07h</td></tr>
<tr><td>H/W Reset</td><td>07h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td colspan="11">
</td></tr>
</table>

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5.3.41. Read Idle Mode Color (81h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
81h	1st	R	0	0	0	0	0	R	G	B	07h

Description

81h: RDIMCOL.

This command returns the current color selection of Idle Mode, see section" Write Idle Mode Color (80h)".

Color selection is defined in the following table:

Idle Mode Color Selection	R	G	B
Black	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

Default setting for color selection for "Normal Black" panel is 'White'; R=G=B:'1'.

Restriction

None

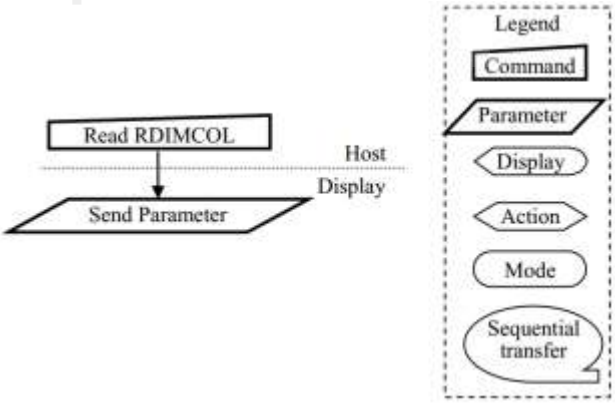
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	07h
S/W Reset	07h
H/W Reset	07h

Flow Chart



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5.3.42. Read DDB Start (A1h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
A1h	1st	R	SID[7:0]								0000h
	2nd	R	SID[15:8]								
	3rd	R	MRID[7:0]								0000h
	4th	R	MRID[15:8]								
	5th	R	1	1	1	1	1	1	1	1	FFh

Description

A1h: RDDDBS (Read DDB Start).

This command reads the supplier identification and display module mode/revision information.

Note: This information is not the same as which "Read ID1 (DAh)", "Read ID2 (DBh)" and "Read ID3 (DCh)" commands return.

Parameter 1: SID[7:0] LCD module's manufacturer ID.

Parameter 2: SID[15:8] LCD module/driver version ID.

Parameter 3: MRID[7:0] LCD module/driver ID.

Parameter 4: MRID[15:8] IC version code.

Parameter 5: FFh - Exit code – there is no more data in the Descriptor Block

This read sequence can be interrupted by any command and it can be continued by the Read DDB Continue (A8h) command. For example, RDDDBS => 1st parameter has been sent => 2nd parameter has been sent => interrupt => RDDDBC => 3rd parameter of the RDDDBS has been sent.

Note: Maximum DDB data length is 4 bytes with OTP program.

Restriction

None

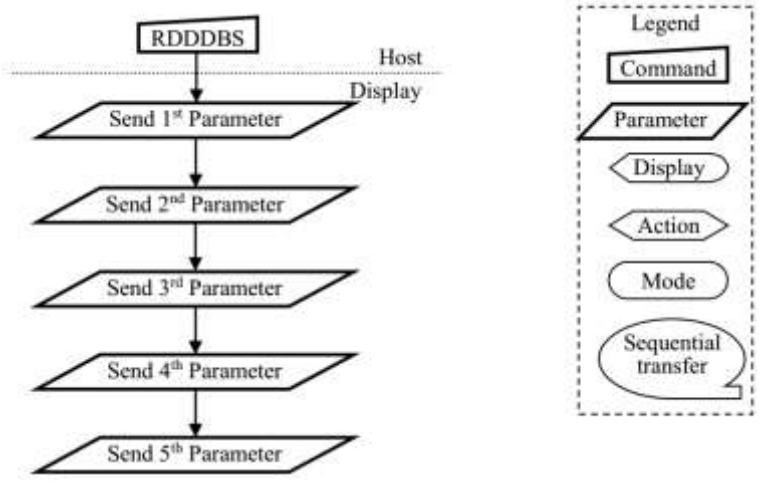
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h_00h_00h_FFh
S/W Reset	00h_00h_00h_00h_FFh
H/W Reset	00h_00h_00h_00h_FFh

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Flow Chart	

first FC components

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5.3.43. Read DDB Continue (A8h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
A8h	1st	R	D1[7:0]								00h
	2nd	R	D2[7:0]								00h
	:	R	:								00h
	Nth	R	Dn[7:0]								00h

Description

A8h: RDDDBC (Read DDB Continue).

This command is used to read the supplier's identification and revision information from the point where RDDDBS (A1h) was interrupted by another command

Restriction

None

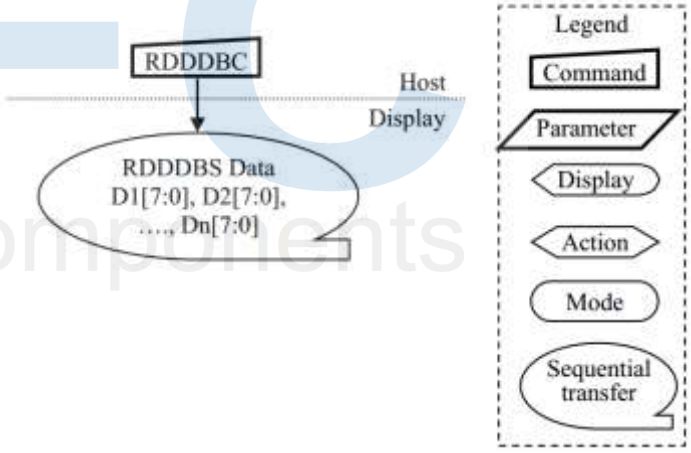
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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5.3.44. Read First Checksum (AAh)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
AAh	1st	R	FCS[7:0]								00h
Description	AAh: RDFCS (Read First Checksum). This command returns the first checksum what has been calculated from Page 0 area registers after the write access to those registers has been done.										
Restriction	It will be necessary to wait 150ms after there is the last write access on Page 0 area registers before there can read this checksum value.										

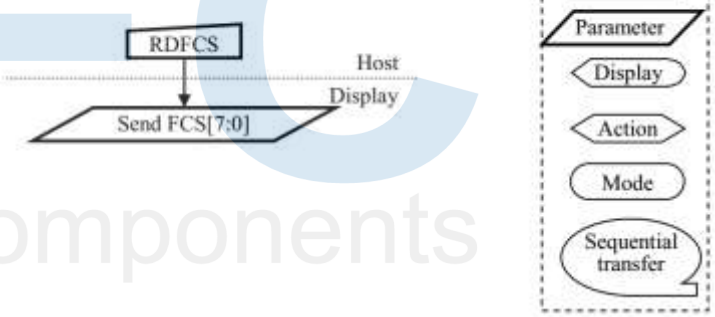
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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5.3.45. Read Continue Checksum (AFh)

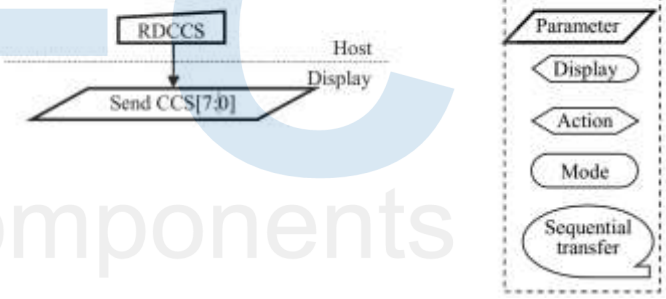
Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
AFh	1st	R	CCS[7:0]								00h
Description	AFh: RDCCS (Read Continue Checksum). This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from Page 0 area registers after the write access to those registers has been done.										
Restriction	It will be necessary to wait 300ms after there is the last write access on Page 0 area registers before there can read this checksum value in the first time.										
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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5.3.46. Read ID1 (DAh)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
DAh	1st	R	ID1[7:0]								00h
Description		Dah: RDID1 (Read ID1). This read byte identifies the display module's manufacturer. The ID1[7:0] is programmed by the OTP function.									
Restriction		None									

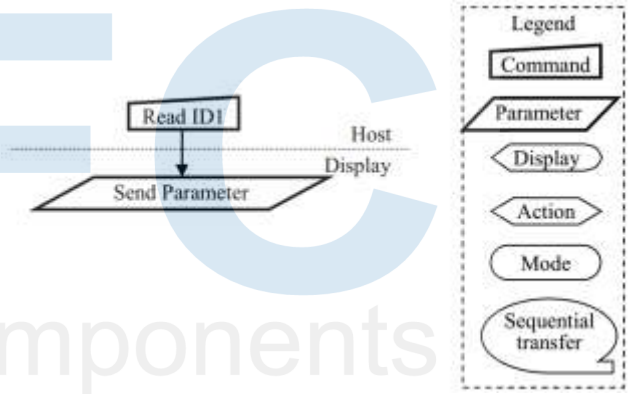
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



first components

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5.3.47. Read ID2 (DBh)

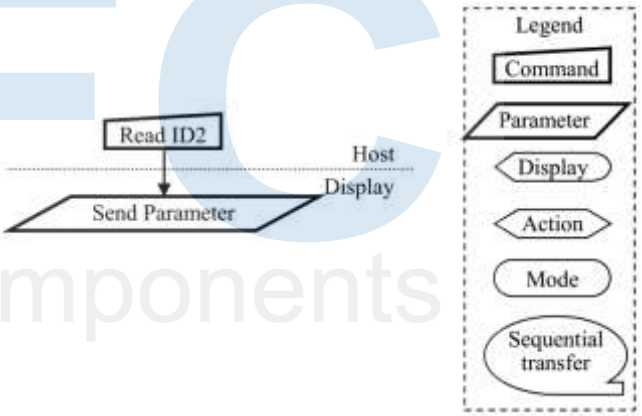
Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
DBh	1st	R	ID2[7:0]								00h
Description	DBh: RDID2 (Read ID2). This read byte is used to track the display module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The ID2[7:0] is programmed by the OTP function.										
Restriction	None										
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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5.3.48. Read ID3 (DCh)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
DCh	1st	R	ID3[7:0]								00h
Description		DCh: RDID3 (Read ID3). This read byte identifies the display module/driver. The ID3[7:0] is programmed by the OTP function.									
Restriction		None									

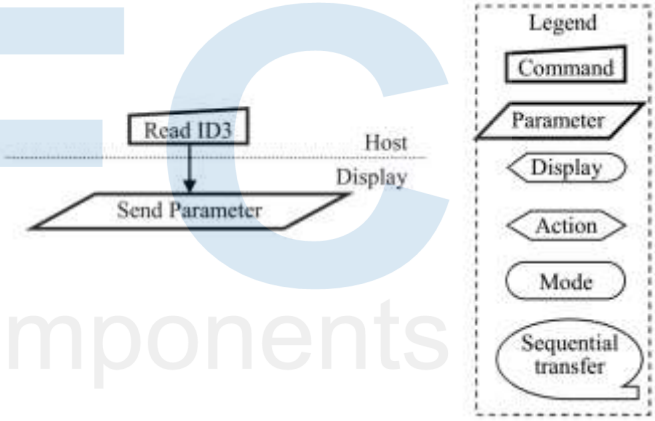
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



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5.3.49. EXTC Command Set Enable Register (FFh)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
FFh	1st	W	1	0	0	1	1	0	0	0	98h
	2nd	W	1	0	0	0	0	0	0	1	81h
	3rd	W	PAGE[7:0]								00h

Description

PAGE[7:0]: Set the command page.

PAGE[7:0]	Command Page
00h	Page 0
01h	Page 1
02h	Page 2
03h	Page 3
04h	Page 4
05h	Page 5
06h	Page 6
07h	Page 7
08h	Page 8
09h	Page 9
0Ah	Page 10
Others	Reserved

Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available

See section "5.1 Command Flow".

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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5.4. Page 1 Command Description

5.4.1. Read ID4 (00h~02h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
00h	1st	R	ID4[23:16]								98h
01h	1st	R	ID4[15:8]								81h
02h	1st	R	ID4[7:0]								1Ch
Description		**ID4[23:0] :** mean the IC model name.									
Restriction		None									
Register Availability			Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes								
Default			Status: Power On Sequence — Default Value: 98h_81h_1Ch Status: S/W Reset — Default Value: 98h_81h_1Ch Status: H/W Reset — Default Value: 98h_81h_1Ch								

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5.4.2. Set Panel Operation Mode and Data Complement Setting (22h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
22h	1st	W/R	0	0	EPF[1:0]		BGR_PANEL	REV_PANEL	SS_PANEL	GS_PANEL	30h

Description

This command defines the panel operation mode

EPF[1:0]: Set the data format from 16/18-bit (R,G,B) to 24-bit (r, g, b) that is mapping into the internal circuit.

See section "4.2.2 16/18-bit Color Data Mapping to 24-bit Pixel Data Operation" for detail description.

BGR_PANEL:

Symbol	Name	Description
BGR_PANEL	Panel RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)

REV_ PANEL: Normally white or normally black panel select.

REV_PANEL	Panel	Data	Color	Source
0	Normally black	0x00	Black	Smallest gamma voltage
		0xFF	White	Largest gamma voltage
1	normally white	0x00	Black	Largest gamma voltage
		0xFF	White	Smallest gamma voltage

SS_ PANEL: Select the shift direction of outputs from the source driver.

SS_PANEL	Source Output Scan Direction
0	Forward
1	Backward

GS_ PANEL: Select the shift direction of outputs from the gate driver.

GS_PANEL	Gate Output Scan Direction
0	Top → Bottom
1	Bottom → Top

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before OTP program)
Power On Sequence	30h
S/W Reset	30h
H/W Reset	30h

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5.4.3. Blanking Porch Control (25h~26h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
25h	1st	W/R	VFP[7:0]								14h
26h	1st	W/R	VBP[7:0]								14h

Description

VFP[7:0] / VBP[7:0]: The VFP[7:0] and VBP[7:0] bits specify the line number of vertical front and back porch period respectively in the Idle Mode.

VFP[7:0] VBP[7:0]	Number of HSYNC of front/back porch (Dec.)
00000000	Setting prohibited
00000001	Setting prohibited
00000010	2
00000011	3
:	:
00001110	14 (VFP[7:0] /VBP[7:0] default)
:	:
11111101	253
11111110	254
11111111	255

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	14h_14h
S/W Reset	14h_14h
H/W Reset	14h_14h

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5.4.4. Touch Synchronization Control (29h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
29h	1st	W/R	0	0	0	0	0	0	0	TOUCH_ VHSYNC	00h
Description		**TOUCH_VHSYNC:** Enable VSOUT / HSOUT signal output.									
Restriction		None									
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

first FC components

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5.4.5. Gate Number (2Eh)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
2Eh	1st	W/R	NL[7:0]								C8h

Description

NL[7:0]: Set the number of lines to drive the LCD at an interval of 4 lines. The number of lines must be the same or more than the number of lines necessary for the size of the LCD panel.

NL[7:0]	The Line Number of the LCD
00h	480
01h	484
02h	488
03h	492
:	:
C5h	1268
C6h	1272
C7h	1276
C8h	1280
Others	Reserved

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	C8h
S/W Reset	C8h
H/W Reset	C8h

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5.4.6. Display Inversion Control (31h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
31h	1st	W/R	0	0	0	0	DINV[3:0]				00h

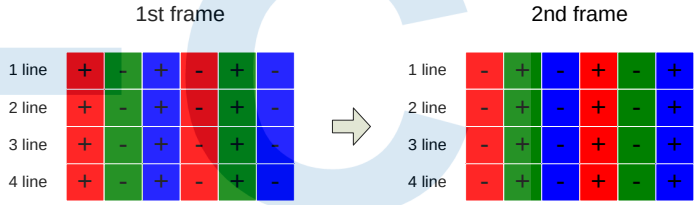
Description

DINV[3:0]: Set Inversion mode

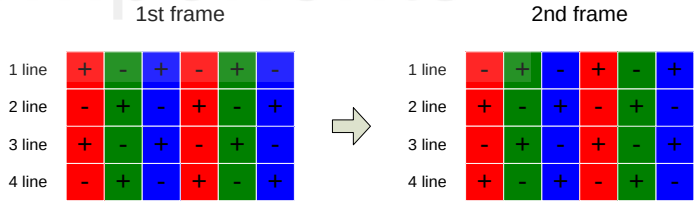
DINV[3:0]	Inversion
0h	Column inversion
1h	1-dot inversion
2h	2-dot inversion
3h	3-dot inversion
4h	4-dot inversion
5h	N/4-dot inversion Note
6h	N/8-dot inversion Note
7h	N/16-dot inversion Note
8h	N/32-dot inversion Note
9h	Zig-Zag inversion Type 1
Ah	Zig-Zag inversion Type 2
Bh	Zig-Zag inversion Type 3
Ch	Zig-Zag inversion Type 4
Others	Reserved

Note : N=The line number of the LCD (setting by NL[7:0])

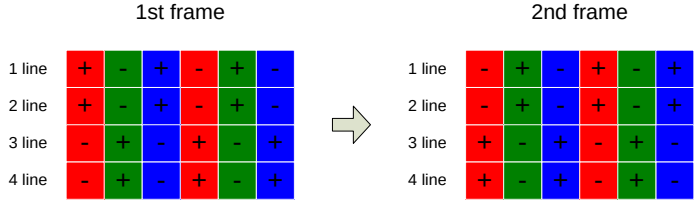
Column Inversion



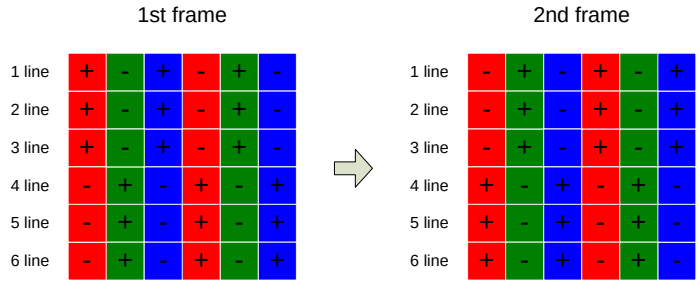
1-Dot Inversion

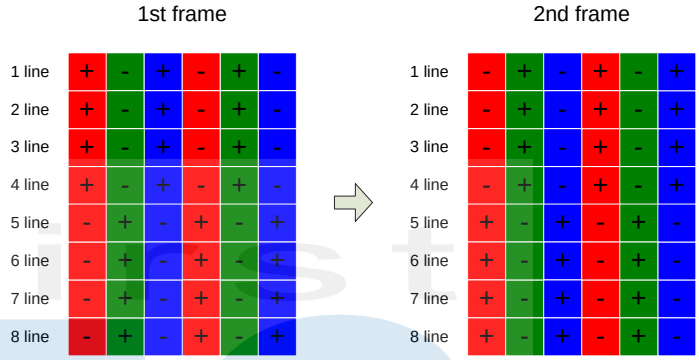


2-Dot Inversion



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<table>
<tr><td></td><td>
3-Dot Inversion


4-Dot Inversion


</td></tr>
<tr><td>Restriction</td><td>None</td></tr>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
</table>

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5.4.7. Dithering Enable (34h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
34h	1st	W/R	0	0	0	0	0	0	0	DITH_EN	00h
Description		**DITH_EN:** 0 : dithering function disable 1 : dithering function enable									
Restriction		None									
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

first FC components

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5.4.8. Pump Clock Adjustment (40h~43h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
40h	1st	W/R	0	EXT_CPCK_SEL[1:0]		1	0	0	VCL_CLK_EN	VGHL_CLK_EN	33h
41h	1st	W/R	0	VCL_CLK_SELA[2:0]			0	VCL_CLK_SELB[2:0]			33h
42h	1st	W/R	0	VGHL_CLK_SELA[2:0]			0	VGHL_CLK_SELB[2:0]			44h
43h	1st	W/R	0	4002_RATIO_FREQA[2:0]			0	4002_RATIO_FREQB[2:0]			55h

Description

EXT_CPCK_SEL[1:0]: Pumping clock control signals selection to external control IC (ILI4003).Set the register before Sleep Out(R11h), when external pumping control be used.

EXT_CPCK_SEL[1:0]	EXTP & EXTN Output
0h	Output x 1.5 waveform
1h	Output x 2 waveform
2h	Output x 3 waveform
3h	Output Low (power down)

VCL_CLK_EN: Enable the pumping cycle of step-up circuit of VCL.

VGHL_CLK_EN: Enable the pumping cycle of step-up circuit of VGH and VGL.

VCL_CLK_SELA[2:0]: Selects the pumping cycle of step-up circuit of VCL in the Normal Mode.

VCL_CLK_SELB[2:0]: Selects the pumping cycle of step-up circuit of VCL in the Idle Mode.

VGHL_CLK_SELA[2:0]: Selects the pumping cycle of step-up circuit of VGH and VGL in the Normal Mode.

VGHL_CLK_SELB[2:0]: Selects the pumping cycle of step-up circuit of VGH and VGL in the Idle Mode.

4002_RATIO_FREQA[2:0]: Selects the pumping cycle of step-up circuit of external control IC (ILI4003) in the Normal Mode.

4002_RATIO_FREQB[2:0]: Selects the pumping cycle of step-up circuit of external control IC (ILI4003) in the Idle Mode.

Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

VGHL_CLK_SELA[2:0], VGHL_CLK_SELB[2:0] VCL_CLK_SELA[2:0], VCL_CLK_SELB[2:0]	Pumping cycle
0h	16H
1h	8H
2h	4H
3h	2H
4h	1H
5h	1/2H
Others	Reserved

4002_RATIO_FREQA[2:0], 4002_RATIO_FREQB[2:0]	Pumping cycle
0h	16H
1h	8H
2h	4H
3h	2H
4h	1H
5h	1/2H
6h	1/4H
7h	1/8H

Restriction	None

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Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	33h_33h_44h_55h
S/W Reset	33h_33h_44h_55h
H/W Reset	33h_33h_44h_55h

first FC components

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5.4.9. Power Control 1 (50h~51h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
50h	1st	W/R	VREG1[7:0]								95h
51h	1st	W/R	VREG2[7:0]								95h

Description

VREG1[7:0]: Set the VREG1OUT voltage for positive Gamma. (12mV/step)

VREG1[7:0]	VREG1OUT voltage (V)
42h	3.504
43h	3.516
44h	3.528
45h	3.540
46h	3.552
47h	3.564
:	:
94h	4.488
95h	4.500
96h	4.512
:	:
E8h	5.496
E9h	5.508
EAh	5.520
:	:
EFh	5.580
F0h	5.592
F1h	5.604
Other	Reserved

VREG2[7:0]: Set the VREG2OUT voltage for negative Gamma. (12mV/step)

VREG2[7:0]	VREG2OUT voltage (V)
42h	-3.564
43h	-3.576
44h	-3.588
45h	-3.600
46h	-3.612
47h	-3.624
:	:
94h	-4.548
95h	-4.560
96h	-4.572
:	:
E8h	-5.556
E9h	-5.568
EAh	-5.580
:	:
EFh	-5.640
F0h	-5.652
F1h	-5.664
Other	Reserved

Restriction	None

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Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>95h_95h</td></tr><tr><td>S/W Reset</td><td>95h_95h</td></tr><tr><td>H/W Reset</td><td>95h_95h</td></tr></table>

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5.4.10. VCOM Control 1 (52h~56h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
52h	1st	W/R	0	0	0	0	0	0	0	VCM1[8]	00h
53h	1st	W/R	VCM1[7:0]								7Bh
54h	1st	W/R	0	0	0	0	0	0	0	VCM2[8]	00h
55h	1st	W/R	VCM2[7:0]								7Bh
56h	1st	R	0	0	0	NVM2	0	0	0	NVM1	00h

Description

VCM1[8:0]: Set the VCOM level used for vertical forward scan (GS_PANEL= 1'b0), when NV memory isn't programmed. (12mV/step)

VCM2[8:0]: Set the VCOM level used for vertical backward scan (GS_PANEL= 1'b1), when NV memory isn't programmed. (12mV/step)

VCM1[8:0] VCM2[8:0]	VCOM voltage (V)
010h	-0.204
011h	-0.216
012h	-0.228
013h	-0.24
014h	-0.252
015h	-0.264
:	:
07Ah	-1.476
07Bh	-1.488
07Ch	-1.5
:	:
149h	-3.96
14Ah	-3.972
14Bh	-3.984
14Ch	-3.996
14Dh	-4.008
Others	Reserved

Note: VCOM ≧ VSN + 0.5V

NVM1 : Selection of the VCM source setting used for vertical forward scan (GS_PANEL= 1'b0). When the NV memory is programmed, the NVM1 will be set as '1' automatically.

0 : Register Page 1 R52h and R53h for VCM setting

1 : Register Page 4 RC4h and RC5h for VCM setting

NVM2 : Selection of the VCM source setting used for vertical backward scan (GS_PANEL= 1'b1). When the NV memory is programmed, the NVM2 will be set as '1' automatically.

0 : Register 54h and 55h for VCM setting

1 : Register Page 4 RC6h and RC7h for VCM setting

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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Default	

Status	Default Value
Power On Sequence	00h_7Bh_00h_7Bh_00h
S/W Reset	00h_7Bh_00h_7Bh_00h
H/W Reset	00h_7Bh_00h_7Bh_00h

first FC components

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5.4.11. Entry Mode Set (58h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
58h	1st	W/R	LVD_EN	0	0	0	0	0	0	0	00h

Description

LVD_EN: Low voltage detection control.

LVD	Low voltage detection
0	Enable
1	Disable

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

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5.4.12. Source Timing Adjust (60h~63h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
60h	1st	W/R	0	0	SDT[5:0]						14h
61h	1st	W/R	0	0	CRT[5:0]						00h
62h	1st	W/R	0	0	EQT[5:0]						19h
63h	1st	W/R	0	0	PCT[5:0]						10h

Description

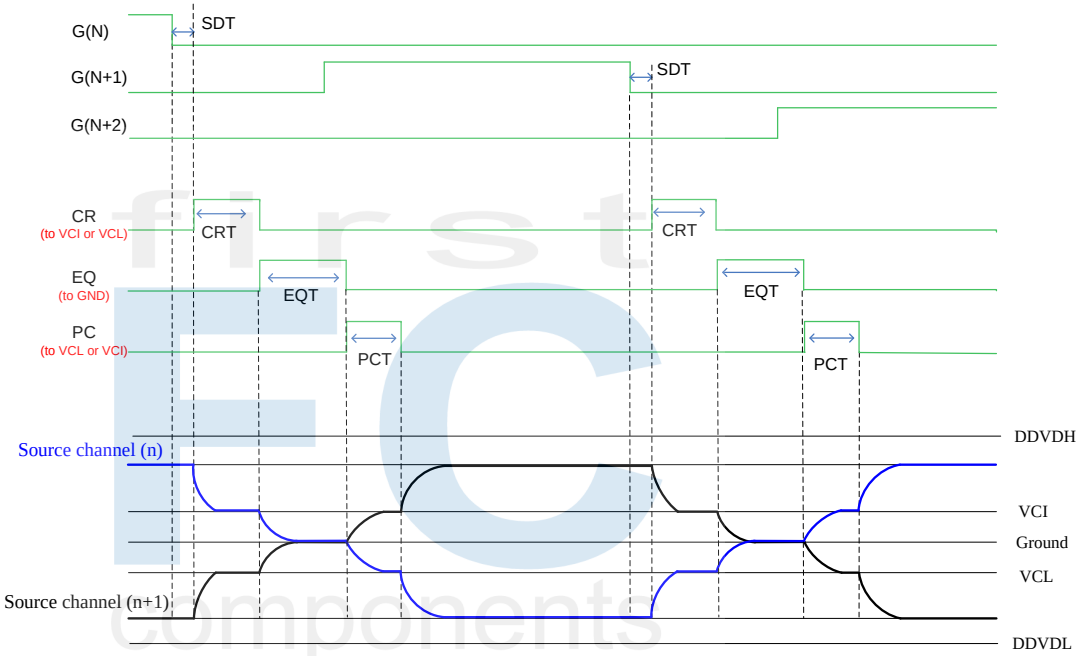
SDT[5:0]: Source SD timing adjustment (time scale: internal T_{OP_CLK}). The timing can be adjusted 0 to 63 time scales.

CRT[5:0]: Source CR timing adjustment (time scale: internal T_{OP_CLK}). The timing can be adjusted 0 to 63 time scales.

EQT[5:0]: Source EQ timing adjustment (time scale: internal T_{OP_CLK}). The timing can be adjusted 8 to 71 time scales.

PCT[5:0]: Source PC timing adjustment (time scale: internal T_{OP_CLK}). The timing can be adjusted 0 to 63 time scales.

Note: T_{OP_CLK}: 62.5ns



Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	14h_00h_19h_10h
S/W Reset	14h_00h_19h_10h
H/W Reset	14h_00h_19h_10h

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5.4.13. Positive Gamma Correction (A0h~B3h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
A0h	1st	W/R	0	0	VP0[5:0]						00h
A1h	1st	W/R	0	VP4[6:0]							0Dh
A2h	1st	W/R	0	VP8[6:0]							1Dh
A3h	1st	W/R	0	0	VP12[5:0]						11h
A4h	1st	W/R	0	0	VP16[5:0]						0Ch
A5h	1st	W/R	0	VP24[6:0]							23h
A6h	1st	W/R	0	0	VP36[5:0]						17h
A7h	1st	W/R	0	0	VP52[5:0]						1Ch
A8h	1st	W/R	VP80[7:0]								82h
A9h	1st	W/R	0	0	VP111[5:0]						21h
AAh	1st	W/R	0	0	VP144[5:0]						2Ah
ABh	1st	W/R	VP175[7:0]								6Bh
ACh	1st	W/R	0	0	VP203[5:0]						19h
ADh	1st	W/R	0	0	VP219[5:0]						14h
AEh	1st	W/R	0	VP231[6:0]							45h
AFh	1st	W/R	0	0	VP239[5:0]						1Dh
B0h	1st	W/R	0	0	VP243[5:0]						23h
B1h	1st	W/R	0	VP247[6:0]							52h
B2h	1st	W/R	0	VP251[6:0]							63h
B3h	1st	W/R	0	0	VP255[5:0]						39h

Description	Set the gray scale voltage to adjust the Gamma characteristics of the TFT panel.
Restriction	None
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h 2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h
S/W Reset	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h 2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h
H/W Reset	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h 2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h

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5.4.14. Pad Control (B6h~B7h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
B6h	1st	W/R	IM_SW_EN	IM_SW[2:0]			RS_SW_EN	0	RS_SW[1:0]		00h
B7h	1st	W/R	0	0	0	0	0	0	LANSEL_SW_EN	LANSEL_SW	00h

Description

IM_SW_EN: Enable/Disable the lane sequence and polarity from internal command setting. The external hardware pin IM[2:0] has no effect when IM_SW_EN is "1".

IM_SW[2:0]: Set the configuration of lane sequence and polarity. (The bottom table is an example for MIPI 4 lane setting)

Internal Pad Control			Configuration of MIPI Lane				
IM_SW2	IM_SW1	IM_SW0	D0P/N Pin	D1P/N Pin	CLKP/N Pin	D2P/N Pin	D3P/N Pin
0	0	0	D3P/N	D2P/N	CLKP/N	D1P/N	D0P/N
0	0	1	D3N/P	D2N/P	CLKN/P	D1N/P	D0N/P
0	1	0	D0P/N	D1P/N	CLKP/N	D2P/N	D3P/N
0	1	1	D0N/P	D1N/P	CLKN/P	D2N/P	D3N/P
1	0	0	D3P/N	D0P/N	CLKP/N	D1P/N	D2P/N
1	0	1	D3N/P	D0N/P	CLKN/P	D1N/P	D2N/P
1	1	0	D2P/N	D1P/N	CLKP/N	D0P/N	D3P/N
1	1	1	D2N/P	D1N/P	CLKN/P	D0N/P	D3N/P

RS_SW_EN: Enable/Disable the resolution from internal command setting. The external hardware pin RS[1:0] has no effect when RS_SW_EN is "1".

RS_SW[1:0]: Set the resolution.

RS_SW1	RS_SW0	Resolution
0	0	800 (RGB) x (480 + (4 x NL)) gate line
0	1	768 (RGB) x (480 + (4 x NL)) gate line
1	0	720 (RGB) x (480 + (4 x NL)) gate line
1	1	Reserved

LANSEL_SW_EN: Enable/Disable the lane number from internal command setting. The external hardware pin LANSEL has no effect when LANSEL_SW_EN is "1".

LANSEL_SW: Set the lane number.

LANSEL_SW="1", MIPI DSI is 2 Lane mode
LANSEL_SW="0", MIPI DSI is 3 or 4 Lane mode

Note: Please reference "Table 2: DSI Interface Lane Mode Selection"

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h
S/W Reset	00h_00h
H/W Reset	00h_00h

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5.4.15. Negative Gamma Correction (C0h~D3h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
C0h	1st	W/R	0	0	VN0[5:0]						00h
C1h	1st	W/R	0	VN4[6:0]							0Dh
C2h	1st	W/R	0	VN8[6:0]							1Dh
C3h	1st	W/R	0	0	VN12[5:0]						11h
C4h	1st	W/R	0	0	VN16[5:0]						0Ch
C5h	1st	W/R	0	VN24[6:0]							23h
C6h	1st	W/R	0	0	VN36[5:0]						17h
C7h	1st	W/R	0	0	VN52[5:0]						1Ch
C8h	1st	W/R	VN80[7:0]								82h
C9h	1st	W/R	0	0	VN111[5:0]						21h
CAh	1st	W/R	0	0	VN144[5:0]						2Ah
CBh	1st	W/R	VN175[7:0]								6Bh
CCh	1st	W/R	0	0	VN203[5:0]						19h
CDh	1st	W/R	0	0	VN219[5:0]						14h
CEh	1st	W/R	0	VN231[6:0]							45h
CFh	1st	W/R	0	0	VN239[5:0]						1Dh
D0h	1st	W/R	0	0	VN243[5:0]						23h
D1h	1st	W/R	0	VN247[6:0]							52h
D2h	1st	W/R	0	VN251[6:0]							63h
D3h	1st	W/R	0	0	VN255[5:0]						39h

Description	Set the gray scale voltage to adjust the Gamma characteristics of the TFT panel.
Restriction	None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h 2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h
S/W Reset	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h 2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h
H/W Reset	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h 2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h

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5.4.16. NV Memory Write (E0h~E2h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
E0h	1st	W/R	PGM_DATA[7:0]								00h
E1h	1st	W/R	PGM_ADR[7:0]								00h
E2h	1st	W/R	PGM_ADR[15:8]								00h

Description

This command is used to program or read the NV memory data.

After a successful OTP operation, the information of PGM_DATA[7:0] will be programmed to the NV memory.

PGM_DATA[7:0]: The programmed data.

PGM_ADR[15:0]: Set the address of the NV memory for programming data. See chapter 15 “NV Memory Programming Flow”.

PGM_ADR[15:0]	Programming data
1h	ID1
2h	ID2
3h	ID3
4h	VCM1[8]
5h	VCM1[7:0]
6h	VCM2[8]
7h	VCM2[7:0]
8h	VREG1[7:0]
9h	VREG2[7:0]
68h~7Bh	REGAM0_P~ REGAM255_P
7Ch~8Fh	REGAM0_N~ REGAM255_N

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h_00h
S/W Reset	00h_00h_00h
H/W Reset	00h_00h_00h

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5.4.17. NV Memory Protection Key (E3h~E5h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
E3h	1st	W/R	KEY[23:16]								00h
E4h	1st	W/R	KEY[15:8]								00h
E5h	1st	W/R	KEY[7:0]								00h
Description		**KEY[23:0]:** NV memory programming protection key. Write an OTP data to PGM_DATA[7:0], this KEY[23:0] must set 0x55AA66h to enable OTP programming. If the KEY[23:0] is not 0x55AA66h, the NV Memory program will be aborted.									
Restriction		None									
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h_00h
S/W Reset	00h_00h_00h
H/W Reset	00h_00h_00h

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5.4.18. NV Memory Status Read (E6h~E9h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
E6h	1st	R	0	ID2_MK[2:0]			0	ID1_MK[2:0]			00h
E7h	1st	R	0	0	0	0	0	ID3_MK[2:0]			00h
E8h	1st	R	GAMMA P_MK	GAMMA N_MK	VCM2_MK[2:0]			VCM1_MK[2:0]			00h
E9h	1st	R	OTP_BU SY	0	0	0	0	0	0	0	00h

Description

These registers uses a mark to record the NV memory programmed time. The bits are increase "+1" automatically after writing the PGM_DATA [7:0] to the NV memory.

ID1_MK[2:0]/ID2_MK[2:0]:

ID1_MK[2:0] / ID2_MK[2:0]			Description
0	0	0	No Programmed
0	0	1	Programmed 1 time already
0	1	1	Programmed 2 times already
1	1	1	Programmed 3 times already

ID3_MK[2:0]:

ID3_MK[2:0]			Description
0	0	0	No Programmed
0	0	1	Programmed 1 time already
0	1	1	Programmed 2 times already
1	1	1	Programmed 3 times already

VCM1_MK[2:0] /VCM2_MK[2:0]:

VCM1_MK[2:0] / VCM2_MK[2:0]			Description
0	0	0	No Programmed
0	0	1	Programmed 1 time already
0	1	1	Programmed 2 times already
1	1	1	Programmed 3 times already

GAMP_MK / GAMN_MK :

GAMP_MK / GAMN_MK	Description
0	No Programmed
1	Programmed 1 time already

OTP BUSY: The status bit of the NV memory programming.

OTP_BUSY	The Status of NV Memory
0	Idle
1	Busy

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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Default	

Status	Default Value
Power On Sequence	00h_00h_00h_00h
S/W Reset	00h_00h_00h_00h
H/W Reset	00h_00h_00h_00h

first FC components

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5.4.19. Time Stamp (F0h~F1h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
F0h	1st	W/R	Time_Stamp_Week[7:0]								00h
F1h	1st	W/R	Time_Stamp_Year[7:0]								00h
Description		This command identifies the display module's manufacture date **Time_Stamp_Week[7:0]:** Week of manufacture. **Time_Stamp_Year[7:0]:** Year of manufacture.									
Restriction											
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h
S/W Reset	00h_00h
H/W Reset	00h_00h

first FC components

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5.4.20. EXTC Command Set Enable Register (FFh)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
FFh	1st	W	1	0	0	1	1	0	0	0	98h
	2nd	W	1	0	0	0	0	0	0	1	81h
	3rd	W	PAGE[7:0]								01h

Description

PAGE[7:0]: Set the command page.

PAGE[7:0]	Command Page
00h	Page 0
01h	Page 1
02h	Page 2
03h	Page 3
04h	Page 4
05h	Page 5
06h	Page 6
07h	Page 7
08h	Page 8
09h	Page 9
0Ah	Page 10
Others	Reserved

Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available

See section "5.1 Command Flow".

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

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5.5. Page 2 Command Description

5.5.1. Dynamic Backlight Control 1 (03h~05h)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
03h	1st	W/R	0	TT_STP_MED[2:0]			1	TT_STP_LOW[2:0]			29h
04h	1st	W/R	0	ST_TIM_LOW[2:0]			0	TT_STP_HIGH[2:0]			14h
05h	1st	W/R	0	ST_TIM_HIGH[2:0]			0	ST_TIM_MED[2:0]			32h

Description

TT_STP_HIGH[2:0]: This parameter is used set the dimming transition step for CABC high enhancement.

TT_STP_MED[2:0]: This parameter is used set the dimming transition step for CABC medium enhancement.

TT_STP_LOW[2:0]: This parameter is used set the dimming transition step for CABC low enhancement.

TT_STP_HIGH[2:0] **TT_STP_MED[2:0]** **TT_STP_LOW[2:0]**	Description
0h	1 step
1h	2 step
2h	4 step
3h	8 step
4h	16 step
5h	32 step
6h	64 step
7h	128 step

ST_TIM_HIGH[2:0]: This parameter is used set the dimming time for CABC high enhancement.

ST_TIM_ MED[2:0]: This parameter is used set the dimming time for CABC medium enhancement.

ST_TIM_ LOW[2:0]: This parameter is used set the dimming time for CABC low enhancement.

ST_TIM_HIGH[2:0] **ST_TIM_MED[2:0]** **ST_TIM_LOW[2:0]**	Description
0h	1 frame
1h	2 frame
2h	4 frame
3h	8 frame
4h	16 frame
5h	32 frame
6h	64 frame
7h	128 frame

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	29h_14h_32h
S/W Reset	29h_14h_32h
H/W Reset	29h_14h_32h

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5.5.2. Dynamic Backlight Control 2 (06h~07h)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
06h	1st	W/R	0	PWM_DUTY_PRECISION[2:0]			0	LEDPWM_POL	LEDON_POL	LEDON	00h
07h	1st	W/R	PWM_DIV[7:0]								0Eh

Description

LEDON: The bit is used to define LEDON enable.

LEDON_POL: The bit is used to define polarity of LEDON.

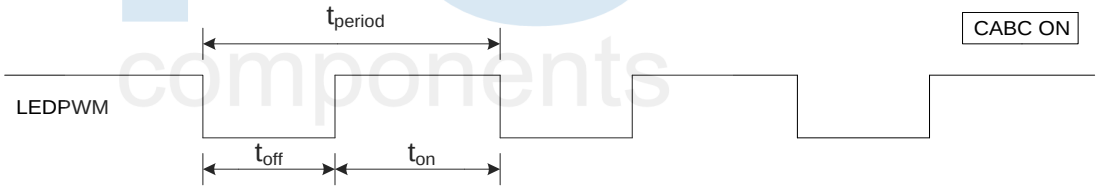
LEDPWM_POL: The bit is used to define polarity of LEDPWM signal.

BL	LEDPWM_POL	LEDPWM pin
0	0	Always low
0	1	Always high
1	0	Original polarity of LEDPWM signal
1	1	Inversed polarity of LEDPWM signal

PWM_DUTY_PRECISION[2:0] / PWM_DIV[7:0]: LEDPWM output period control. This command is used to adjust the PWM waveform period of PWM_OUT. The PWM period is calculated using the following equation.

$$f_{LEDPWM} = \frac{32\ MHz}{(\text{PWM_DIV}[7:0]+1) \times PWM_DUTY_PRECISION}$$

PWM_DUTY_PRECISION[2:0]	*PWM_DUTY_PRECISION*	$f_{LEDPWM\ (MAX)}$ (PWM_DIV[7:0]=0)	$f_{LEDPWM\ (min)}$ (PWM_DIV[7:0]=255)
0h	4096	7.8 KHz	31 Hz
1h	2048	15.6 KHz	61 Hz
2h	1024	31.2 KHz	122 Hz
3h	512	62.5 KHz	244 Hz
4h	256	125 KHz	488 Hz
5h~7h	Reserved	X	X



Note : The output frequency tolerance of internal frequency divider in CABC is ±10%

X = void.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_0Eh
S/W Reset	00h_0Eh
H/W Reset	00h_0Eh

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5.5.3. IIE Function Control (10h~19h)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
10h	1st	W/R	0	0	0	0	0	PRT_EN	SKIN_EN	0	06h
11h	1st	W/R	0	AUTO_MEAN	0	0	CN_EN	CN_INV	SHP_EN	0	00h
12h	1st	W/R	0	0	0	0	0	0	CN_LV[1:0]		02h
13h	1st	W/R	0	0	1	0	SRE_MIDIV_LV[1:0]		0	0	20h
15h	1st	W/R	RGB_MEAN[7:0]								80h
16h	1st	W/R	SRE_HYSTERESIS_EN	0	0	SRE_DIM_EN	SRE_SC_EN	SRE_CE_EN	0	0	1Ch
17h	1st	W/R	0	SRE_OFFS[2:0]			0	SRE_DIM_STP[2:0]			01h
18h	1st	W/R	SRE_DIM_FRAME[7:0]								08h
19h	1st	W/R	SRE_SC_GAIN_ADJ[2:0]			SRE_HYSTERESIS_LIMIT[4:0]					C0h

Description

PRT_EN: Enable the over-saturation protection of saturation enhancement.

SKIN_EN: Enable the skin-tone protection of saturation enhancement.

AUTO_MEAN: Enable auto image mean calculation RGB_MEAN[7:0] is not available when AUTO_MEAN=1h.

CN_EN: Enable contrast enhancement.

CN_INV: Select contrast enhancement Function.

CN_INV	Contrast Function
0	Contrast increase
1	Contrast decrease

SHP_EN: Enable sharpness enhancement.

CN_LV[1:0] : Define contrast enhancement level.

SRE_MIDIV_LV[1:0] : Define SRE medium level enhancement select.

SRE_MIDIV_LV[1:0]	Enhancement level
00h / 11h	Level_M
01h	Level_H
10h	Level_L

RGB_MEAN[7:0]: Setting image mean value, available when AUTO_MEAN=0h.

SRE_HYSTERESIS_EN: SRE hysteresis mode enable signal.

SRE_DIM_EN: SRE dimming function enable signal.

SRE_SC_EN: SRE saturation compensation enable.

SRE_CE_EN: SRE contrast enhancement enable.

SRE_OFFS[2:0]: SRE offset value

SRE_DIM_STP[2:0]: Setting the number of dimming steps for transition

SRE_DIM_STP[2:0]	Description
0h	2 step
1h	4 step
2h	8 step
3h	16 step
4h	32 step
5h	64 step
6h	128 step
7h	256 step

SRE_DIM_FRAME[7:0]: Setting the step time as frame units for each dimming step

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	<table><tr><th>SRE_DIM_FRAME[7:0]</th><th>Description</th></tr><tr><td>0h~2h</td><td>2 frame</td></tr><tr><td>3</td><td>4 frame</td></tr><tr><td>4</td><td>4 frame</td></tr><tr><td>5</td><td>5 frame</td></tr><tr><td>6</td><td>6 frame</td></tr><tr><td>:</td><td>:</td></tr><tr><td>:</td><td>:</td></tr><tr><td>254</td><td>254 frame</td></tr><tr><td>255</td><td>255 frame</td></tr></table> **SRE_SC_GAIN_ADJ[2:0]:** SRE saturation compensation gain value **SRE_HYSTERESIS_LIMIT[4:0]:** SRE hysteresis limit value when hysteresis mode on
Restriction	None
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>06h_00h_02h_20h_80h_1Ch_01h_08h_C0h</td></tr><tr><td>S/W Reset</td><td>06h_00h_02h_20h_80h_1Ch_01h_08h_C0h</td></tr><tr><td>H/W Reset</td><td>06h_00h_02h_20h_80h_1Ch_01h_08h_C0h</td></tr></table>

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5.5.4. IIE Saturation Enhancement Control 1 (1Ah~1Ch)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1Ah	1st	W/R	0	0	SE_RATIO_L[5:0]						07h
1Bh	1st	W/R	0	0	SE_RATIO_M[5:0]						09h
1Ch	1st	W/R	0	0	SE_RATIO_H[5:0]						0Ch

Description

SE_RATIO_L[5:0]: Define low saturation enhancement level of User Command 55h (Page0_R55h).

SE_RATIO_M[5:0]: Define medium saturation enhancement level of User Command 55h (Page0_R55h).

SE_RATIO_H[5:0]: Define high saturation enhancement level of User Command 55h (Page0_R55h).

$$Saturation_{enhanced} = Saturation_{original} + (Saturation_{original} \times SE_RATIO)$$

SE_RATIO_L[5:0] SE_RATIO_M[5:0] SE_RATIO_H[5:0]	Ratio (Dec)	SE_RATIO_L[5:0] SE_RATIO_M[5:0] SE_RATIO_H[5:0]	Ratio (Dec)
00h	0.0	10h	1.0
01h	0.0625	11h	1.0625
02h	0.125	12h	1.125
03h	0.1875	13h	1.1875
04h	0.25	14h	1.25
05h	0.3125	15h	1.3125
06h	0.375	16h	1.375
07h	0.4375	17h	1.4375
08h	0.5	18h	1.5
09h	0.5625	19h	1.5625
0Ah	0.625	1Ah	1.625
0Bh	0.6875	1Bh	1.6875
0Ch	0.75	1Ch	1.75
0Dh	0.8125	1Dh	1.8125
0Eh	0.875	1Eh	1.875
0Fh	0.9375	1Fh	1.9375

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	07h_09h_0Ch
S/W Reset	07h_09h_0Ch
H/W Reset	07h_09h_0Ch

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5.5.5. IIE Saturation Protection Control (40h~4Fh)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
40h	1st	W/R	0	0	0	LEVEL0_SR[4:0]					02h
41h	1st	W/R	0	0	0	LEVEL1_SR[4:0]					04h
42h	1st	W/R	0	0	0	LEVEL2_SR[4:0]					06h
43h	1st	W/R	0	0	0	LEVEL3_SR[4:0]					08h
44h	1st	W/R	0	0	0	LEVEL4_SR[4:0]					0Ah
45h	1st	W/R	0	0	0	LEVEL5_SR[4:0]					0Ch
46h	1st	W/R	0	0	0	LEVEL6_SR[4:0]					0Eh
47h	1st	W/R	0	0	0	LEVEL7_SR[4:0]					0Eh
48h	1st	W/R	0	0	0	LEVEL8_SR[4:0]					0Ch
49h	1st	W/R	0	0	0	LEVEL9_SR[4:0]					0Ah
4Ah	1st	W/R	0	0	0	LEVEL10_SR[4:0]					08h
4Bh	1st	W/R	0	0	0	LEVEL11_SR[4:0]					06h
4Ch	1st	W/R	0	0	0	LEVEL12_SR[4:0]					04h
4Dh	1st	W/R	0	0	0	LEVEL13_SR[4:0]					03h
4Eh	1st	W/R	0	0	0	LEVEL14_SR[4:0]					02h
4Fh	1st	W/R	0	0	0	LEVEL15_SR[4:0]					00h

Description

This register is used to restrict the enhancement gain of saturation enhancement. This function is able to use when PRT_EN=1.

LEVEL0_SR[4:0]: Adjust the weight value of saturation steps 0~15.

LEVEL1_SR[4:0]: Adjust the weight value of saturation steps 16~31.

LEVEL2_SR[4:0]: Adjust the weight value of saturation steps 32~47.

LEVEL3_SR[4:0]: Adjust the weight value of saturation steps 48~63.

LEVEL4_SR[4:0]: Adjust the weight value of saturation steps 64~79.

LEVEL5_SR[4:0]: Adjust the weight value of saturation steps 80~95.

LEVEL6_SR[4:0]: Adjust the weight value of saturation steps 96~111.

LEVEL7_SR[4:0]: Adjust the weight value of saturation steps 128~143.

LEVEL8_SR[4:0]: Adjust the weight value of saturation steps 144~159.

LEVEL9_SR[4:0]: Adjust the weight value of saturation steps 160~175.

LEVEL10_SR[4:0]: Adjust the weight value of saturation steps 176~191.

LEVEL11_SR[4:0]: Adjust the weight value of saturation steps 192~207.

LEVEL12_SR[4:0]: Adjust the weight value of saturation steps 208~223.

LEVEL13_SR[4:0]: Adjust the weight value of saturation steps 224~239.

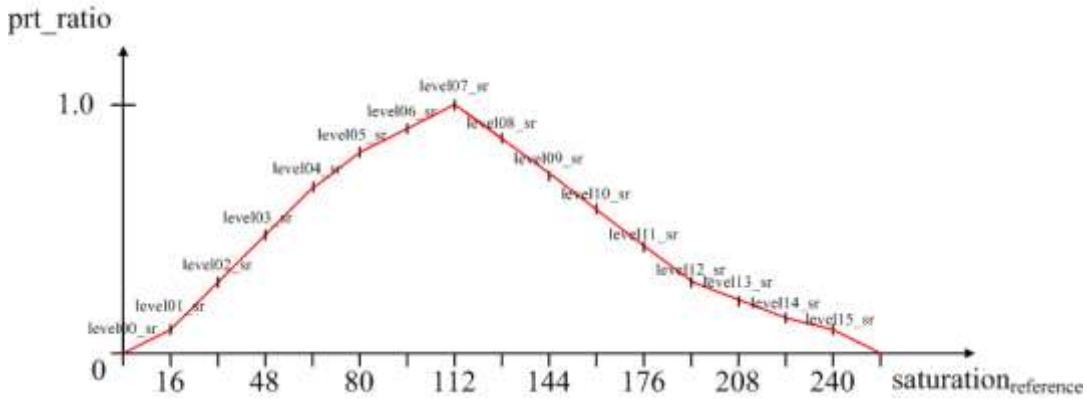
LEVEL14_SR[4:0]: Adjust the weight value of saturation steps 240~255.

LEVEL15_SR[4:0]: Adjust the weight value of saturation steps 256.

$$Saturation_{enhanced} = Saturation_{original} + (Saturation_{original} \times SE_RATIO \times PRT_RATIO)$$

$$PRT_RATIO = 0 \sim 1.0$$

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<table>
<tr><td></td><td>
</td></tr>
<tr><td>Restriction</td><td>None</td></tr>
<tr><td>Register
Availability</td><td><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td><table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>02h_04h_06h_08h_0Ah_0Ch_0Eh_0Eh_0Ch_0Ah_08h_06h_04h_03h_02h_00h</td></tr>
<tr><td>S/W Reset</td><td>02h_04h_06h_08h_0Ah_0Ch_0Eh_0Eh_0Ch_0Ah_08h_06h_04h_03h_02h_00h</td></tr>
<tr><td>H/W Reset</td><td>02h_04h_06h_08h_0Ah_0Ch_0Eh_0Eh_0Ch_0Ah_08h_06h_04h_03h_02h_00h</td></tr>
</table></td></tr>
</table>

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5.5.6. IIE Sharpness Enhancement Control (5Ah~5Ch)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
5Ah	1st	W/R	0	0	0	SHP_RATIO[4:0]					18h
5Bh	1st	W/R	SHP_THR_H[7:0]								64h
5Ch	1st	W/R	SHP_THR_L[7:0]								1Eh

Description

This register sets the enhancement level of the sharpness enhancement. This function is able to use when SHP_EN=1

SHP_RATIO[4:0]: Adjust the ratio of sharpness enhancement.

$$Y_{enh} = Y_{org} + (Y_{org} – blur(Y_{org})) \times SHP_RATIO$$

SHP_RATIO[4:0]	Ratio (Dec)	SHP_RATIO[4:0]	Ratio (Dec)
00h	0.0	10h	2.0
01h	0.125	11h	2.125
02h	0.25	12h	2.25
03h	0.375	13h	2.375
04h	0.5	14h	2.5
05h	0.625	15h	2.625
06h	0.75	16h	2.75
07h	0.875	17h	2.875
08h	1.0	18h	3.0
09h	1.125	19h	3.125
0Ah	1.25	1Ah	3.25
0Bh	1.375	1Bh	3.375
0Ch	1.5	1Ch	3.5
0Dh	1.625	1Dh	3.625
0Eh	1.75	1Eh	3.75
0Fh	1.875	1Fh	3.875

SHP_THR_H[7:0]: Define Sharpness enhancement upper bound threshold.

SHP_THR_L[7:0]: Define Sharpness enhancement lower bound threshold.

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	18h_64h_1Eh
S/W Reset	18h_64h_1Eh
H/W Reset	18h_64h_1Eh

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5.5.7. IIE Contrast Enhancement Control (60h~66h)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
60h	1st	W/R	0	0	CN_00[5:0]						0Eh
61h	1st	W/R	0	0	CN_01[5:0]						18h
62h	1st	W/R	0	0	CN_02[5:0]						24h
63h	1st	W/R	0	0	CN_03[5:0]						28h
64h	1st	W/R	0	0	CN_04[5:0]						24h
65h	1st	W/R	0	0	CN_05[5:0]						18h
66h	1st	W/R	0	0	CN_06[5:0]						0Eh

Description

This register sets the weight value of the turning point of contrast gain cure. This function is able to use when CN_EN=1

CN_00[5:0]: Adjust the weight of S curve ratio of turning point 1.

CN_01[5:0]: Adjust the weight of S curve ratio of turning point 2.

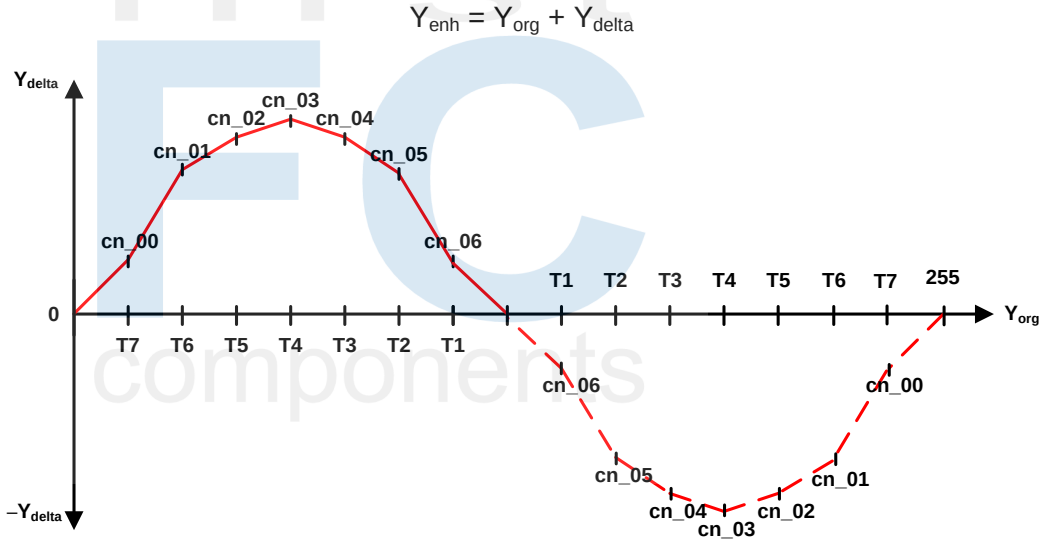
CN_02[5:0]: Adjust the weight of S curve ratio of turning point 3.

CN_03[5:0]: Adjust the weight of S curve ratio of turning point 4.

CN_04[5:0]: Adjust the weight of S curve ratio of turning point 5.

CN_05[5:0]: Adjust the weight of S curve ratio of turning point 6.

CN_06[5:0]: Adjust the weight of S curve ratio of turning point 7.



Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0Eh_18h_24h_28h_24h_18h_0Eh
S/W Reset	0Eh_18h_24h_28h_24h_18h_0Eh
H/W Reset	0Eh_18h_24h_28h_24h_18h_0Eh

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5.5.8. EXTC Command Set Enable Register (FFh)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
FFh	1st	W	1	0	0	1	1	0	0	0	98h
	2nd	W	1	0	0	0	0	0	0	1	81h
	3rd	W	PAGE[7:0]								02h

Description

PAGE[7:0]: Set the command page.

PAGE[7:0]	Command Page
00h	Page 0
01h	Page 1
02h	Page 2
03h	Page 3
04h	Page 4
05h	Page 5
06h	Page 6
07h	Page 7
08h	Page 8
09h	Page 9
0Ah	Page 10
Others	Reserved

Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available

See section "5.1 Command Flow".

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	02h
S/W Reset	02h
H/W Reset	02h

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5.6. Page 3 Command Description

5.6.1. EXTC Command Set Enable Register (FFh)

Command Page			Page 3								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
FFh	1st	W	1	0	0	1	1	0	0	0	98h
	2nd	W	1	0	0	0	0	0	0	1	81h
	3rd	W	PAGE[7:0]								03h

Description

PAGE[7:0]: Set the command page.

PAGE[7:0]	Command Page
00h	Page 0
01h	Page 1
02h	Page 2
03h	Page 3
04h	Page 4
05h	Page 5
06h	Page 6
07h	Page 7
08h	Page 8
09h	Page 9
0Ah	Page 10
Others	Reserved

Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available

See section "5.1 Command Flow".

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	03h
S/W Reset	03h
H/W Reset	03h

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5.7. Page 4 Command Description

5.7.1. DSI Lanes Control (00h)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
00h	1st	W/R	MIPI_LANE_SEL	0	0	0	0	0	0	0	80h
Description			**MIPI_LANE_SEL:** MIPI DSI lane number selection *Note: When use this setting, please reference to chapter 4.1 "DSI System Interface".*								
Restriction			None								
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	80h
S/W Reset	80h
H/W Reset	80h

first FC components

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5.7.2. SSC Function (0Bh,0Eh)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
0Bh	1st	W/R	SSC_DIG_EN	SSC_DIG_STEP[2:0]			0	0	0	0	00h
0Eh	1st	W/R	SSC_DIG_CNT[7:0]								00h

Description

SSC_DIG_EN : Enable/disable the SSC(Spread Spectrum Clock) function.

SSC_DIG_STEP[2:0] : Set SSC parameter.

SSC_DIG_CNT[7:0] : Set SSC parameter.

SSC	Address 0Bh	Address 0Eh
±1%	80h	17h
±2%	90h	0Bh
Others	Reserved	Reserved

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h
S/W Reset	00h_00h
H/W Reset	00h_00h

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5.7.3. Charge-Pump Setting (21h)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
21h	1st	W/R	DMY_PUMP	0	1	1	0	0	0	0	B0h

Description

DMY_PUMP: Control the driver behavior when host stop transferring video data.

DMY_PUMP	Description
0	Charge-Pump VGH/VGL keep pumping and display shows smallest gamma voltage
1	Charge-Pump VGH/VGL keep pumping

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	B0h
S/W Reset	B0h
H/W Reset	B0h

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5.7.4. Idle Mode Frame Rate (23h)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
23h	1st	W/R	RTNB[7:0]								2Dh
Description			**RTNB[7:0]:** Used for adjusting frame rate of idle mode by the following rule: One idle frame time = (VACT + VFP + VBP) * (62.5ns * RTNB) VACT (the line number of the LCD) is defined at “5.4.5 Gate Number (2Eh)”. VFP and VBP are defined at “5.4.3 Blanking Porch Control (25h~26h)”.								
Restriction			None								
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	2Dh
S/W Reset	2Dh
H/W Reset	2Dh

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5.7.5. Internal SD Timing Control (26h)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
26h	1st	W/R	DET_TOLERANCE_OP[3:0]				0	1	1	0	76h

Description

DET_TOLERANCE_OP[3:0]: Control internal SD timing between latch1 load into latch2.

DET_TOLERANCE_OP[3:0]	Description
0000	62.5ns x 1
0001	62.5ns x 2
…	…
1111	62.5ns x 16

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	76h
S/W Reset	76h
H/W Reset	76h

first FC components

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5.7.6. Touch Synchronization Timing Adjust (27h~2Ah)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
27h	1st	W/R	TOUCH_OPT[1:0]		VSOD[1:0]		HSOM[1:0]		HFP_HBP_OPT	VS_PW_OPT	00h
28h	1st	W/R	HSOD[7:0]								05h
29h	1st	W/R	HSOHW[7:0]								19h
2Ah	1st	W/R	VS_OUT_EN	HS_OUT_EN	VS_OUT_POL	HS_OUT_POL	0	0	STB_EN	0	F0h

Description

This command controls the synchronization output. This function is able to use when Page1_R29h=01h.

TOUCH_OPT[1:0]: Select the Output Mode of synchronization (time scale: internal T_{OP_CLK})

TOUCH_OPT[1:0]	Description
0h	Off
1h	VFP+VBP
2h	Adjustable for VSOUT / HSOUT(Note 2)
3h	VFP+VBP / HFP+HBP

VSOD[1:0]: Set the VSOUT delay timing (time scale: internal T_{OP_CLK})

VSOD[1:0]	Description
0h	0 line (First line of back porch)
1h	1 line
2h	2 line
3h	3 line

HSOM[1:0]: Set the HSOUT active period (time scale: internal T_{OP_CLK})

HSOM[1:0]	Description
0h	VACT Period + VFP + VBP
1h	VACT Period
2h	VFP+VBP
3h	Reserved

HFP_HBP_OPT: Select the output source for HSOUT

HFP_HBP_OPT	Description
0	Prebuf-Source
1	HSOUT(Note 2)

VS_PW_OPT: Set the pulse width of VSOUT

VS_PW_OPT	Description
0	pulse width = 1H
1	During transition from display off to display on : pulse width = 3H During transition from display on to display off : pulse width = 2H Otherwise : pulse width = 1H

HSOD[7:0]: Set HSOUT delay timing (time scale: internal T_{OP_CLK})

HSOD[1:0]	Description
0h	0clk
1h	1clk
2h	2clk
:	:
FDh	253clk
FEh	254clk
FFh	255clk

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HSOHW[7:0]: Set the high width of HSOUT (time scale: internal T_{OP_CLK})

HSOHW[1:0]	Description
0h	Reserved
1h	1clk
2h	2clk
:	:
FDh	253clk
FEh	254clk
FFh	255clk

VS_OUT_EN: VS signal output enable (1: enable, 0: disable)

HS_OUT_EN: HS signal output enable (1: enable, 0: disable)

VS_OUT_POL: VS signal polarity (1: non-inversion, 0: inversion)

HS_OUT_POL: HS signal polarity (1: non-inversion, 0: inversion)

STB_EN: touch option

Note 1: T_{OP_CLK}: 32ns

Note 2: When use this setting, please reference to chapter 17 "Touch Synchronization Signal".

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_05h_19h_F0h
S/W Reset	00h_05h_19h_F0h
H/W Reset	00h_05h_19h_F0h

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5.7.7. BIST Mode Function (2Dh,2Fh)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
2Dh	1st	W/R	FRM_PT[7:0]								FFh
2Fh	1st	W/R	0	0	FRM_CYC[1:0]		0	0	0	FRM_EN	00h

Description

FRM_PT[7:0]: Enable/disable the pattern

FRM_PT[7:0]	Pattern
FRM_PT[0]	White
FRM_PT[1]	Black
FRM_PT[2]	Red
FRM_PT[3]	Green
FRM_PT[4]	Blue
FRM_PT[5]	Gray128
FRM_PT[6]	Gray127
FRM_PT[7]	V-Color bar

See also sections:"8 BIST Mode Function "

FRM_CYC[1:0]: Set scan cycle of each pattern

FRM_CYC[1:0]	Description
0h	64 frames
1h	128 frames
2h	256 frames
3h	512 frames

FRM_EN: Enable/disable BIST mode function

FRM_EN	Description
0	Normal display
1	Enable BIST mode

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	FFh_00h
S/W Reset	FFh_00h
H/W Reset	FFh_00h

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5.7.8. Source Timing Setting (35h)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
35h	1st	W/R	0	0	0	1	HZ_OPT	1	1	1	17h

Description

HZ_OPT: Maximum source OP drive time.

HZ_OPT	Description
0	Disable
1	Enable (Before enable this function , set Page4_R3Ah_D[7]=0)

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	17h
S/W Reset	17h
H/W Reset	17h

first FC components

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5.7.9. Power Saving Control (3Ah)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
3Ah	1st	W/R	PS_EN	PCST[6:0]							A4h

Description

PS_EN: Source power saving enable

PS_EN	Description
0	Disable
1	Enable

PCST[6:0]: Control power saving period

PCST[6:0]	Description
0000000	62.5ns x 1
0000001	62.5ns x 2
0000010	62.5ns x 3
…	…
0100100	62.5ns x 37
Others	Inhibited

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	A4h
S/W Reset	A4h
H/W Reset	A4h

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5.7.10. Power Control 1 (69h)

<table>
<tr><th colspan="2">Command Page</th><th colspan="10">Page 4</th></tr>
<tr><th>Address</th><th>Parameter</th><th>W/R</th><th>D7</th><th colspan="3">D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>69h</td><td>1st</td><td>W/R</td><td>1</td><td colspan="3">CP_VCL_CLP_OPTION_PRE[2:0]</td><td></td><td></td><td>0</td><td>1</td><td>1</td><td>1</td><td>D7h</td></tr>
<tr><td>Description</td><td colspan="13">CP_VCL_CLP_OPTION_PRE[2:0]: Set VCL clamp level.
<table>
<tr><th>CP_VCL_CLP_OPTION_PRE[2:0]</th><th>VCL clamp level (V)</th></tr>
<tr><td>0h</td><td>-3.0V</td></tr>
<tr><td>1h</td><td>-2.9V</td></tr>
<tr><td>2h</td><td>-2.8V</td></tr>
<tr><td>3h</td><td>-2.7V</td></tr>
<tr><td>4h</td><td>-2.6V</td></tr>
<tr><td>5h</td><td>-2.5V</td></tr>
<tr><td>6h</td><td>-2.4V</td></tr>
<tr><td>7h</td><td>-2.3V</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>D7h</td></tr>
<tr><td>S/W Reset</td><td>D7h</td></tr>
<tr><td>H/W Reset</td><td>D7h</td></tr>
</table></td></tr>
</table>

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5.7.11. Power Control 2 (6Eh)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
6Eh	1st	W/R	0	DI_PWR_REG	REG1_VRH_CP[5:0]						6Ah

Description

DI_PWR_REG: Select the input power mode.

DI_PWR_REG	BOOSTM2	BOOSTM1	BOOSTM0	Note
0	0	0	1	Power Mode 2A External VDDI, VSP and VSN (VCI=VSP) Note 1
1	0	0	1	Power Mode 4 External VDDI, VCI, VSP and VSN
X	0	1	0	Power Mode 3 External VDDI and VCI (ILI4003)
prohibited				-

Note 1: VCI and VSP pads must be connected by external metal path.

REG1_VRH_CP[5:0]: Set VGH clamp level. (0.18V/step)

REG1_VRH_CP[5:0]	VGH clamp level (V)
03h	7.98
04h	8.16
05h	8.34
06h	8.52
07h	8.7
08h	8.88
:	:
29h	14.82
2Ah	15
2Bh	15.18
:	:
39h	17.7
3Ah	17.88
3Bh	18.06
Other	Reserved

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	6Ah
S/W Reset	6Ah
H/W Reset	6Ah

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5.7.12. Power Control 3 (6Fh)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
6Fh	1st	W/R	VGLREG_EN_GO	DI_CP_VGH_BH[2:0]			DI_CP_VGL_BL[2:0]			DI_CP_VCL_REG_SEL	34h

Description

VGLREG_EN_GO: Enable/Disable VGL regulator circuit (VGLO1).

VGLREG_EN_GO	VGL regulator
0	Disable
1	Enable

DI_CP_VGH_BH[2:0]: Set the factor used in the step-up circuits for VGH.

Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

DI_CP_VGH_BH[2:0]	VGH Output (power mode 3, 4)	VGH Output (power mode 2A)	Flying Capacitor
0h	Reserved	Reserved	-
1h	2*VSP	2*VSP	C21P/N + C22P/N (option)
2h	2.5*VSP	3*VSP	C21P/N + C22P/N (option)
3h	3*VSP	3*VSP	C21P/N + C22P/N (option)
4h	3.5*VSP	4*VSP	C21P/N + C22P/N
5h	4*VSP	4*VSP	C21P/N + C22P/N
6h	4.5*VSP	5*VSP	C21P/N + C22P/N
7h	5*VSP	5*VSP	C21P/N + C22P/N

DI_CP_VGL_BL[2:0]: Set the factor used in the step-up circuits for VGL. Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

DI_CP_VGL_BL[2:0]	VGL Output (power mode 3, 4)	VGL Output (power mode 2A)	Flying Capacitor
0h	-1.5*VSP	-2*VSP	C23P/N + C24P/N (option)
1h	-2*VSP	-2*VSP	C23P/N + C24P/N (option)
2h	-2.5*VSP	-3*VSP	C23P/N + C24P/N (option)
3h	-3*VSP	-3*VSP	C23P/N + C24P/N (option)
4h	-3.5*VSP	-4*VSP	C23P/N + C24P/N
5h	-4*VSP	-4*VSP	C23P/N + C24P/N
6h	-4.5*VSP	-5*VSP	C23P/N + C24P/N
7h	-5*VSP	-5*VSP	C23P/N + C24P/N

DI_CP_VCL_REG_SEL: Set VCL power source.

DI_CP_VCL_REG_SEL	VCL power source
0	Charge-pumping circuit (Connect the C41P/C41N and C42P/C42N capacitor)
1	Regulator circuit (Disconnect the C41P/C41N and C42P/C42N capacitor)

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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Default	

Status	Default Value
Power On Sequence	34h
S/W Reset	34h
H/W Reset	34h

first FC components

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5.7.13. VREG1/2 Setting (7Ah)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
7Ah	1st	W/R	0	0	0	DI_REG_REG1_EN_CAP	0	0	0	0	00h

Description

DI_REG_REG1_EN_CAP: Using VREG1/2 external caps(1uF) enable

DI_REG_REG1_EN_CAP	Description
1	IC uses VREG1/2 caps(1uF) at FPC
0	IC doesn't use VREG1/2 caps(1uF) at FPC

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

first FC components

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5.7.14. LVD Function 1 (87h)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
87h	1st	W/R	DI_LVD_CTL[3:0]				1	0	1	0	BAh

Description

DI_LVD_CTL[3:0]: The sensitivity adjustment of detecting when battery is removed and power voltage is low.

DI_LVD_CTL[3:0]	Description
1111	sensitivity high
1011	sensitivity medium
0010	sensitivity low
0000	disable detecting
Others	Inhibited

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	BAh
S/W Reset	BAh
H/W Reset	BAh

first FC components

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5.7.15. LVD Function 2 (88h)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
88h	1st	W/R	DIS_LVD_CHK	0	0	0	1	0	1	1	8Bh

Description

DIS_LVD_CHK: LVD check function control.

DIS_LVD_CHK	Description
0	When LVD is detected, IC will directly turn off pump power and go into sleep in sequence
1	When LVD is detected, IC will go into normal power-off/sleep in sequence

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8Bh
S/W Reset	8Bh
H/W Reset	8Bh

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5.7.16. VCOM Control (8Bh)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
8Bh	1st	W/R	1	1	1	0	DI_VCM_SEL0_EN	0	1	1	E3h

Description

DI_VCM_SEL0_EN: Set the VCOM output mode.

DI_VCM_SEL0_EN	GS_PANEL Note	VCOM output mode
0	0	Set VCOM level by VCM1[8:0]
0	1	Set VCOM level by VCM2[8:0]
1	0	VCOM = 0V
1	1	VCOM = 0V

Note: Please reference"5.4.2 Set Panel Operation Mode and Data Complement Setting (22h)"

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	E3h
S/W Reset	E3h
H/W Reset	E3h

first components

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5.7.17. Power Control 4 (8Ch~8Dh)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
8Ch	1st	W/R	0	DI_VCOM_REG_VGLREG[6:0]							03h
8Dh	1st	W/R	0	DI_VCOM_CP_VGLCLP[6:0]							14h

Description

DI_VCOM_REG_VGLREG[6:0]: Set VGLO1 voltage adjustment. (0.18V/step)

DI_VCOM_REG_VGLREG[6:0]	VGLO1 voltage (V)
03h	-6.99
04h	-7.17
05h	-7.35
06h	-7.53
07h	-7.71
08h	-7.89
09h	-8.07
0Ah	-8.25
0Bh	-8.43
0Ch	-8.61
0Dh	-8.79
0Eh	-8.97
0Fh	-9.15
10h	-9.33
11h	-9.51
12h	-9.69
13h	-9.87
14h	-10.05
15h	-10.23
:	:
3Fh	-17.79
40h	-17.97
41h	-18.15
Others	Reserved

DI_VCOM_CP_VGLCLP[6:0]: Set VGL clamp level. (0.18V/step)

DI_VCOM_CP_VGLCLP[6:0]	VGL clamp level (V)
03h	-6.99
04h	-7.17
05h	-7.35
06h	-7.53
07h	-7.71
08h	-7.89
09h	-8.07
0Ah	-8.25
0Bh	-8.43
0Ch	-8.61
0Dh	-8.79
0Eh	-8.97
0Fh	-9.15
10h	-9.33
11h	-9.51
12h	-9.69
13h	-9.87
14h	-10.05

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		15h	-10.23
		:	:
		3Fh	-17.79
		40h	-17.97
		41h	-18.15
		Others	Reserved
Restriction	None		
Register Availability			

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	03h_14h
S/W Reset	03h_14h
H/W Reset	03h_14h

first FC components

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5.7.18. Reload Gamma Setting (B2h)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
B2h	1st	W/R	RELOAD_GMA_EN	RELOAD_GMA_LINE8_EN	0	1	0	0	0	1	D1h

Description

RELOAD_GMA_EN: Gamma setting reload enable when IC operates at sleep-out state.

RELOAD_GMA_EN	Description
0	Disable
1	Enable

RELOAD_GMA_LINE8_EN: Gamma setting reload at the period of 8 line when IC operates at sleep-out state.

RELOAD_GMA_LINE8_EN	Description
0	Disable
1	Enable

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	D1h
S/W Reset	D1h
H/W Reset	D1h

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5.7.19. Gamma Bias Level (B5h)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
B5h	1st	W/R	0	0	0	0	0	DI_GMA_GAP[2:0]			02h

Description

DI_GMA_GAP[2:0]: Control the gamma bias level.

DI_GMA_GAP[2:0]	Description
111	High
110	Medium High
010	Default value
Others	inhibited

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	02h
S/W Reset	02h
H/W Reset	02h

first FC components

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5.7.20. Temperature Detecting Setting 1 (BBh~C2h)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
BBh	1st	W/R	EN_TEMP_PROCESS	0	CP_VGH_TAP_C[5:0]						1Eh
BCh	1st	W/R	0	0	CP_VGH_TAP_L[5:0]						1Eh
BDh	1st	W/R	0	0	CP_VGH_TAP_M[5:0]						1Eh
BEh	1st	W/R	0	0	CP_VGH_TAP_H[5:0]						1Eh
BFh	1st	W/R	VCOM_C[7:0]								4Ch
C0h	1st	W/R	VCOM_L[7:0]								4Ch
C1h	1st	W/R	VCOM_M[7:0]								4Ch
C2h	1st	W/R	VCOM_H[7:0]								4Ch

Description

EN_TEMP_PROCESS / EN_TS: Enable/Disable Temperature Detecting function.

EN_TEMP_PROCESS	EN_TS	Function
0	0	Disable
1	1	Enable
Other		Reserved

CP_VGH_TAP_C[5:0]: Set VGH clamp level for Temp_Cold. (0.18V/step)

CP_VGH_TAP_L[5:0]: Set VGH clamp level for Temp_Low. (0.18V/step)

CP_VGH_TAP_M[5:0]: Set VGH clamp level for Temp_Middle. (0.18V/step)

CP_VGH_TAP_H[5:0]: Set VGH clamp level for Temp_High. (0.18V/step)

CP_VGH_TAP_C[5:0] CP_VGH_TAP_L[5:0] CP_VGH_TAP_M[5:0] CP_VGH_TAP_H[5:0]	VGH clamp level (V)
03h	7.98
04h	8.16
05h	8.34
06h	8.52
07h	8.7
08h	8.88
:	:
28h	14.64
29h	14.82
2Ah	15
2Bh	15.18
2Ch	15.36
:	:
37h	17.34
38h	17.52
39h	17.7
3Ah	17.88
3Bh	18.06
Other	Reserved

VCOM_C[8:0]: Set the VCOM level for Temp_Cold.

VCOM_L[8:0]: Set the VCOM level for Temp_Low.

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VCOM_M[8:0]: Set the VCOM level for Temp_Middle.

VCOM_H[8:0]: Set the VCOM level for Temp_High.

VCOM_C[8:0] VCOM_L[8:0] VCOM_M[8:0] VCOM_H[8:0]	VCOM voltage (V)
010h	-0.204
011h	-0.216
012h	-0.228
013h	-0.24
014h	-0.252
015h	-0.264
:	:
07Ah	-1.476
07Bh	-1.488
07Ch	-1.5
:	:
149h	-3.96
14Ah	-3.972
14Bh	-3.984
14Ch	-3.996
14Dh	-4.008
Others	Reserved

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	1Eh_1Eh_1Eh_1Eh_4Ch_4Ch_4Ch_4Ch
S/W Reset	1Eh_1Eh_1Eh_1Eh_4Ch_4Ch_4Ch_4Ch
H/W Reset	1Eh_1Eh_1Eh_1Eh_4Ch_4Ch_4Ch_4Ch

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5.7.21. Read VCOM OTP Data (C4h~C7h)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
C4h	1st	R	0	0	0	0	0	0	0	OTP_VCM1[8]	00h
C5h	1st	R	OTP_VCM1[7:0]								7Bh
C6h	1st	R	0	0	0	0	0	0	0	OTP_VCM2[8]	00h
C7h	1st	R	OTP_VCM2[7:0]								7Bh

Description

OTP_VCM1[8:0]: Read the VCOM1 OTP data used for vertical forward scan (GS_PANEL= 1'b0), when NV memory is programmed. (12mV/step)

OTP_VCM2[8:0]: Read the VCOM2 OTP data used for vertical backward scan (GS_PANEL= 1'b1), when NV memory is programmed. (12mV/step)

OTP_VCM1[8:0] OTP_VCM2[8:0]	VCOM voltage (V)
010h	-0.204
011h	-0.216
012h	-0.228
013h	-0.24
014h	-0.252
015h	-0.264
:	:
07Ah	-1.476
07Bh	-1.488
07Ch	-1.5
:	:
149h	-3.96
14Ah	-3.972
14Bh	-3.984
14Ch	-3.996
14Dh	-4.008
Others	Reserved

Note: VCOM ≧ VSN + 0.5V

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_7Bh_00h_7Bh
S/W Res t	00h_7Bh_00h_7Bh
H/W Reset	00h_7Bh_00h_7Bh

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5.7.22. Temperature Detecting Setting 2 (C8h~CEh)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
C8h	1st	W/R	TS_TH0[7:0]								00h
C9h	1st	W/R	TS_TH1[7:0]								00h
CAh	1st	W/R	TS_TH2[7:0]								00h
CBh	1st	W/R	TS_TH3[7:0]								00h
CCh	1st	W/R	TS_TH0[9:8]		TS_TH1[9:8]		TS_TH2[9:8]		TS_TH3[9:8]		00h
CDh	1st	W/R	TS_DEBT_OPT[3:0]				TS_HYST_OPT[3:0]				02h
CEh	1st	W/R	EN_TS	VCOM_C[8]	VCOM_L[8]	VCOM_M[8]	VCOM_H[8]	1	0	0	04h

Description

TS_TH0[9:0]: Set the temperature detecting range threshold for Temp_Cold.

TS_TH1[9:0]: Set the temperature detecting range threshold for Temp_Low.

TS_TH2[9:0]: Set the temperature detecting range threshold for Temp_Middle.

TS_TH3[9:0]: Set the temperature detecting range threshold for Temp_High.

TS_DEBT_OPT[3:0]: Set the de-bounce of temperature detecting range.

TS_HYST_OPT[3:0]: Set the hysteresis of temperature detecting range.

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h_00h_00h_00h_02h_04h
S/W Reset	00h_00h_00h_00h_00h_02h_04h
H/W Reset	00h_00h_00h_00h_00h_02h_04h

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5.7.23. OTP Control (D7h)

<table>
<tr><th colspan="2">Command Page</th><th colspan="10">Page 4</th></tr>
<tr><th>Address</th><th>Parameter</th><th>W/R</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>D7h</td><td>1st</td><td>W/R</td><td>0</td><td>0</td><td>0</td><td>OTP_PATH</td><td colspan="2">PROG_SEL[1:0]</td><td>0</td><td>0</td><td>1Ch</td></tr>
<tr><td>Description</td><td colspan="11">OTP_PATH:
<table><tr><th>OTP_PATH</th><th>Description</th></tr><tr><td>0</td><td>Internal VGH Programming</td></tr><tr><td>1</td><td>External MTP_PWR Programming</td></tr></table>PROG_SEL[1:0]:
<table><tr><th>PROG_SEL[1:0]</th><th>Description</th></tr><tr><td>0h</td><td>Inhibited</td></tr><tr><td>1h</td><td>Internal Programming Setting (Best Setting)</td></tr><tr><td>2h</td><td>Inhibited</td></tr><tr><td>3h</td><td>Internal Programming Setting (Default)</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="11">None</td></tr>
<tr><td>Register Availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>1Ch</td></tr><tr><td>S/W Reset</td><td>1Ch</td></tr><tr><td>H/W Reset</td><td>1Ch</td></tr></table></td></tr>
</table>

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5.7.24. EXTC Command Set Enable Register (FFh)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
FFh	1st	W	1	0	0	1	1	0	0	0	98h
	2nd	W	1	0	0	0	0	0	0	1	81h
	3rd	W	PAGE[7:0]								04h

Description

PAGE[7:0]: Set the command page.

PAGE[7:0]	Command Page
00h	Page 0
01h	Page 1
02h	Page 2
03h	Page 3
04h	Page 4
05h	Page 5
06h	Page 6
07h	Page 7
08h	Page 8
09h	Page 9
0Ah	Page 10
Others	Reserved

Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available

See section "5.1 Command Flow".

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	04h
S/W Reset	04h
H/W Reset	04h

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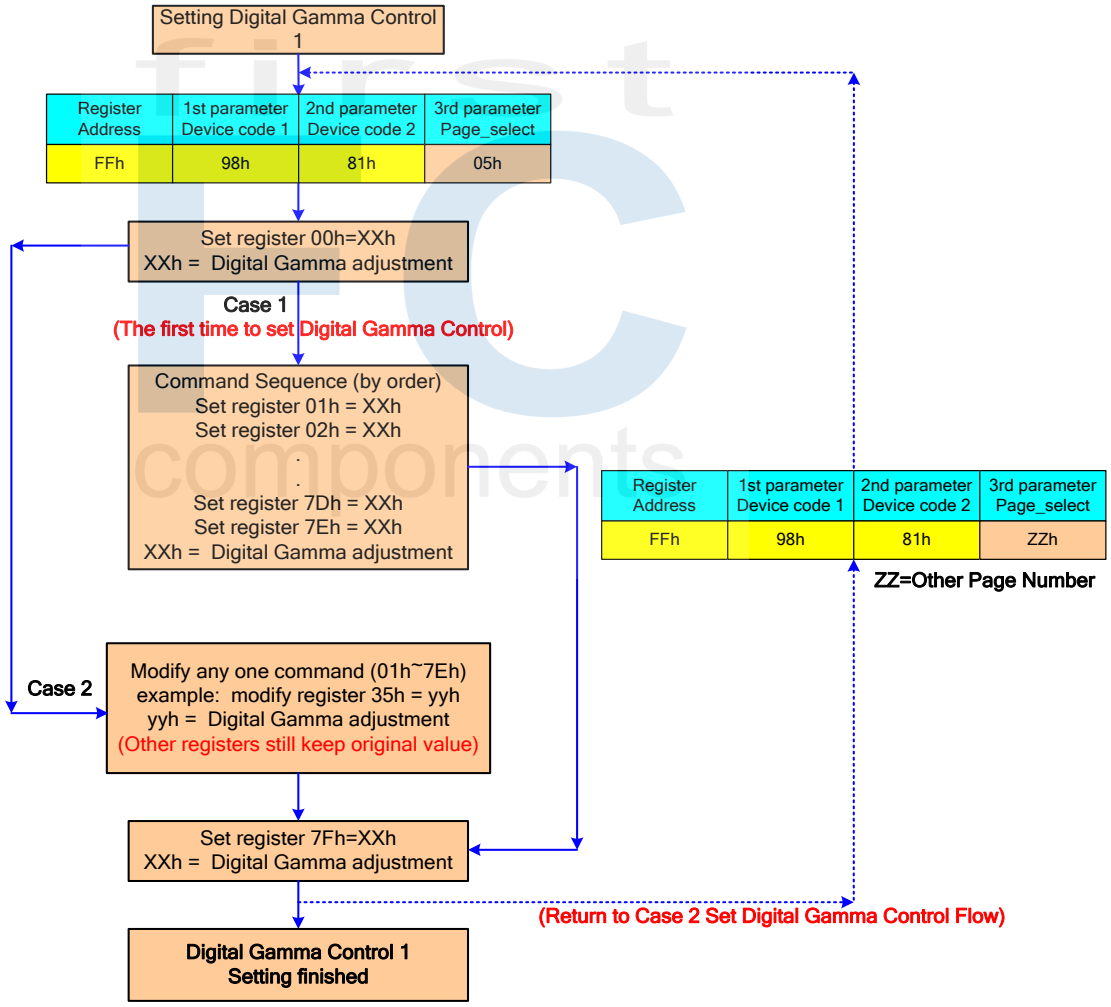
5.8. Page 5 Command Description

5.8.1. Fine Digital Gamma Control 1 (00h~7Fh)

Command Page			Page 5								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	1st	W	RDIN0[7:0]								00h
01h	1st	W	RDIN1[7:0]								00h
02h	1st	W	RDIN2[7:0]								00h
03h	1st	W	RDIN3[7:0]								00h
04h	1st	W	RDIN4[7:0]								00h
05h	1st	W	RDIN5[7:0]								00h
:	1st	W	:								00h
7Ah	1st	W	RDIN122[7:0]								00h
7Bh	1st	W	RDIN123[7:0]								00h
7Ch	1st	W	RDIN124[7:0]								00h
7Dh	1st	W	RDIN125[7:0]								00h
7Eh	1st	W	RDIN126[7:0]								00h
7Fh	1st	W	RDIN127[7:0]								00h

Description

RDINx[7:0]: Digital Gamma Macro-adjustment registers for red gamma curve.



Restriction	None

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Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	00h_00h_...00h_00h
S/W Reset	00h_00h_...00h_00h
H/W Reset	00h_00h_...00h_00h

first FC components

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5.8.2. Digital 3 Gamma Enable (80h)

Command Page			Page 5								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
80h	1st	W/R	0	0	0	0	0	0	0	EN_3G	00h
Description		**En_3G:** 0 : digital 3 gamma disable 1 : digital 3 gamma enable									
Restriction		None									
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before OTP program)
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

first FC components

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5.8.3. EXTC Command Set Enable Register (FFh)

Command Page			Page 5								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
FFh	1st	W	1	0	0	1	1	0	0	0	98h
	2nd	W	1	0	0	0	0	0	0	1	81h
	3rd	W	PAGE[7:0]								05h

Description

PAGE[7:0]: Set the command page.

PAGE[7:0]	Command Page
00h	Page 0
01h	Page 1
02h	Page 2
03h	Page 3
04h	Page 4
05h	Page 5
06h	Page 6
07h	Page 7
08h	Page 8
09h	Page 9
0Ah	Page 10
Others	Reserved

Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available

See section "5.1 Command Flow".

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	05h
S/W Reset	05h
H/W Reset	05h

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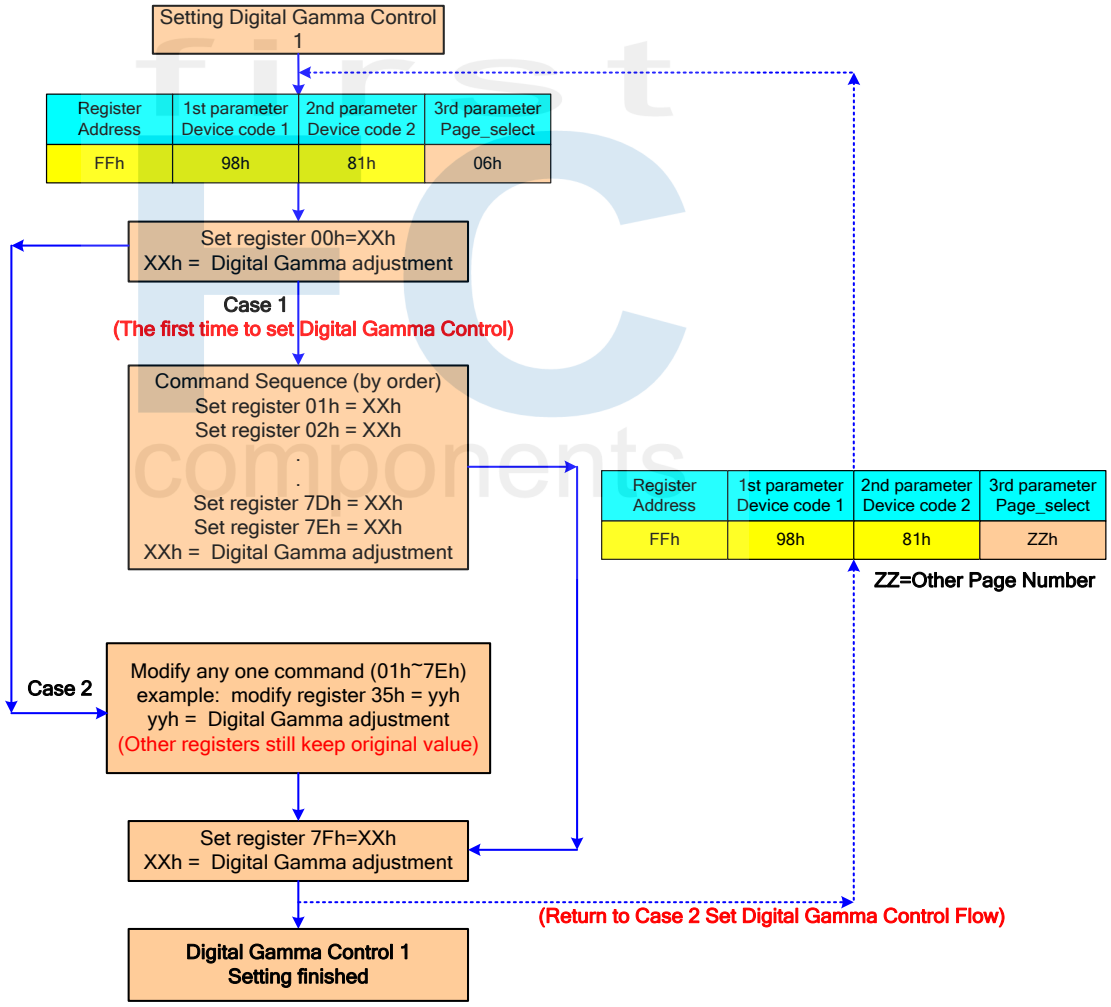
5.9. Page 6 Command Description

5.9.1. Fine Digital Gamma Control 2 (00h~7Fh)

Command Page			Page 6								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	1st	W	RDIN128[7:0]								00h
01h	1st	W	RDIN129[7:0]								00h
02h	1st	W	RDIN130[7:0]								00h
03h	1st	W	RDIN131[7:0]								00h
04h	1st	W	RDIN132[7:0]								00h
05h	1st	W	RDIN133[7:0]								00h
:	1st	W	:								00h
7Ah	1st	W	RDIN250[7:0]								00h
7Bh	1st	W	RDIN251[7:0]								00h
7Ch	1st	W	RDIN252[7:0]								00h
7Dh	1st	W	RDIN253[7:0]								00h
7Eh	1st	W	RDIN254[7:0]								00h
7Fh	1st	W	RDIN255[7:0]								00h

Description

RDINx[7:0]: Digital Gamma Macro-adjustment registers for red gamma curve.



Restriction	None

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Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Sleep In / Yes
Default	Status / Default Value Power On Sequence / 00h_00h_...00h_00h S/W Reset / 00h_00h_...00h_00h H/W Reset / 00h_00h_...00h_00h

first FC components

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5.9.2. EXTC Command Set Enable Register (FFh)

Command Page			Page 6								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
FFh	1st	W	1	0	0	1	1	0	0	0	98h
	2nd	W	1	0	0	0	0	0	0	1	81h
	3rd	W	PAGE[7:0]								06h

Description

PAGE[7:0]: Set the command page.

PAGE[7:0]	Command Page
00h	Page 0
01h	Page 1
02h	Page 2
03h	Page 3
04h	Page 4
05h	Page 5
06h	Page 6
07h	Page 7
08h	Page 8
09h	Page 9
0Ah	Page 10
Others	Reserved

Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available

See section "5.1 Command Flow".

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	06h
S/W Reset	06h
H/W Reset	06h

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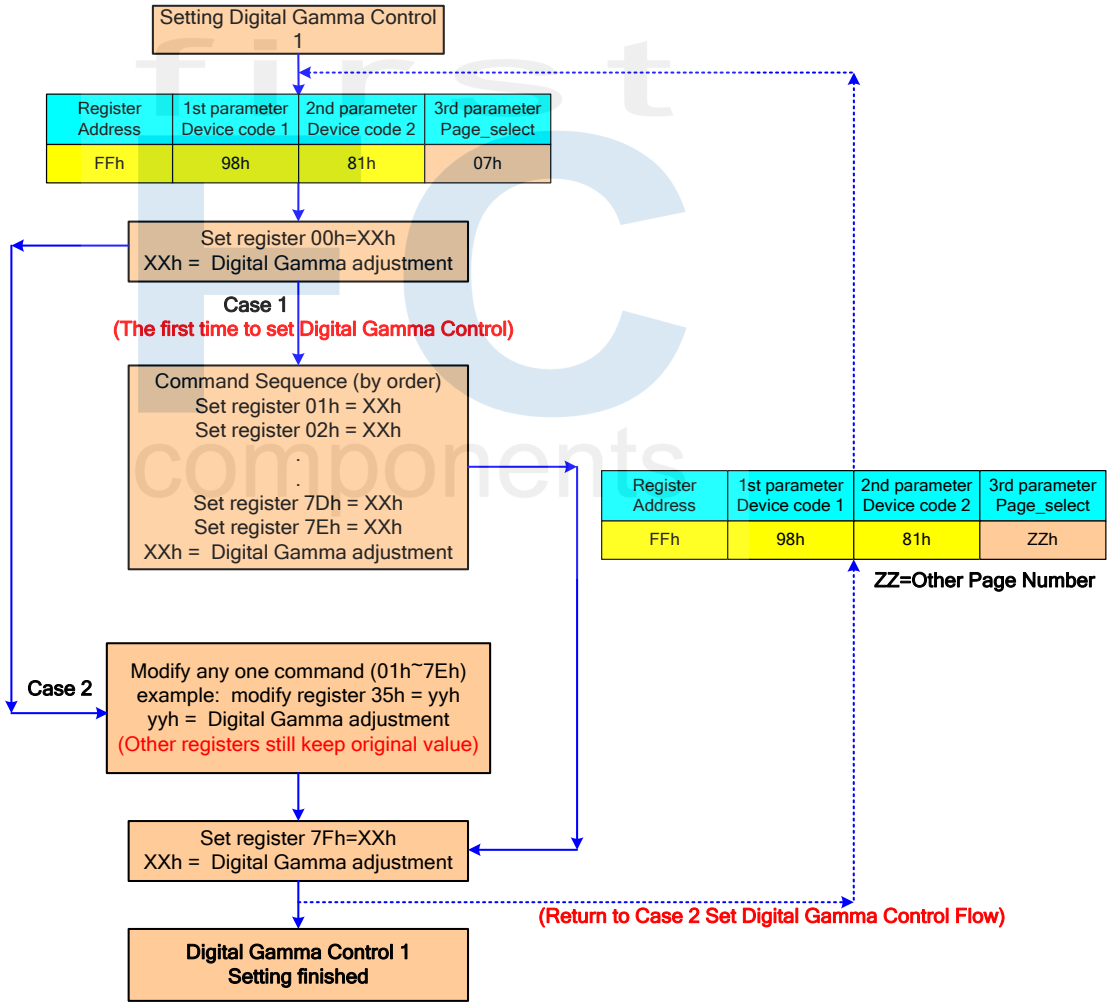
5.10. Page 7 Command Description

5.10.1. Fine Digital Gamma Control 3 (00h~7Fh)

Command Page			Page 7								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	1st	W	GDIN0[7:0]								00h
01h	1st	W	GDIN1[7:0]								00h
02h	1st	W	GDIN2[7:0]								00h
03h	1st	W	GDIN3[7:0]								00h
04h	1st	W	GDIN4[7:0]								00h
05h	1st	W	GDIN5[7:0]								00h
:	1st	W	:								00h
7Ah	1st	W	GDIN122[7:0]								00h
7Bh	1st	W	GDIN123[7:0]								00h
7Ch	1st	W	GDIN124[7:0]								00h
7Dh	1st	W	GDIN125[7:0]								00h
7Eh	1st	W	GDIN126[7:0]								00h
7Fh	1st	W	GDIN127[7:0]								00h

Description

GDINx[7:0]: Digital Gamma Macro-adjustment registers for green gamma curve.



Restriction	None

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Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	00h_00h_...00h_00h
S/W Reset	00h_00h_...00h_00h
H/W Reset	00h_00h_...00h_00h

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5.10.2. EXTC Command Set Enable Register (FFh)

Command Page			Page 7								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
FFh	1st	W	1	0	0	1	1	0	0	0	98h
	2nd	W	1	0	0	0	0	0	0	1	81h
	3rd	W	PAGE[7:0]								07h

Description

PAGE[7:0]: Set the command page.

PAGE[7:0]	Command Page
00h	Page 0
01h	Page 1
02h	Page 2
03h	Page 3
04h	Page 4
05h	Page 5
06h	Page 6
07h	Page 7
08h	Page 8
09h	Page 9
0Ah	Page 10
Others	Reserved

Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available

See section "5.1 Command Flow".

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	07h
S/W Reset	07h
H/W Reset	07h

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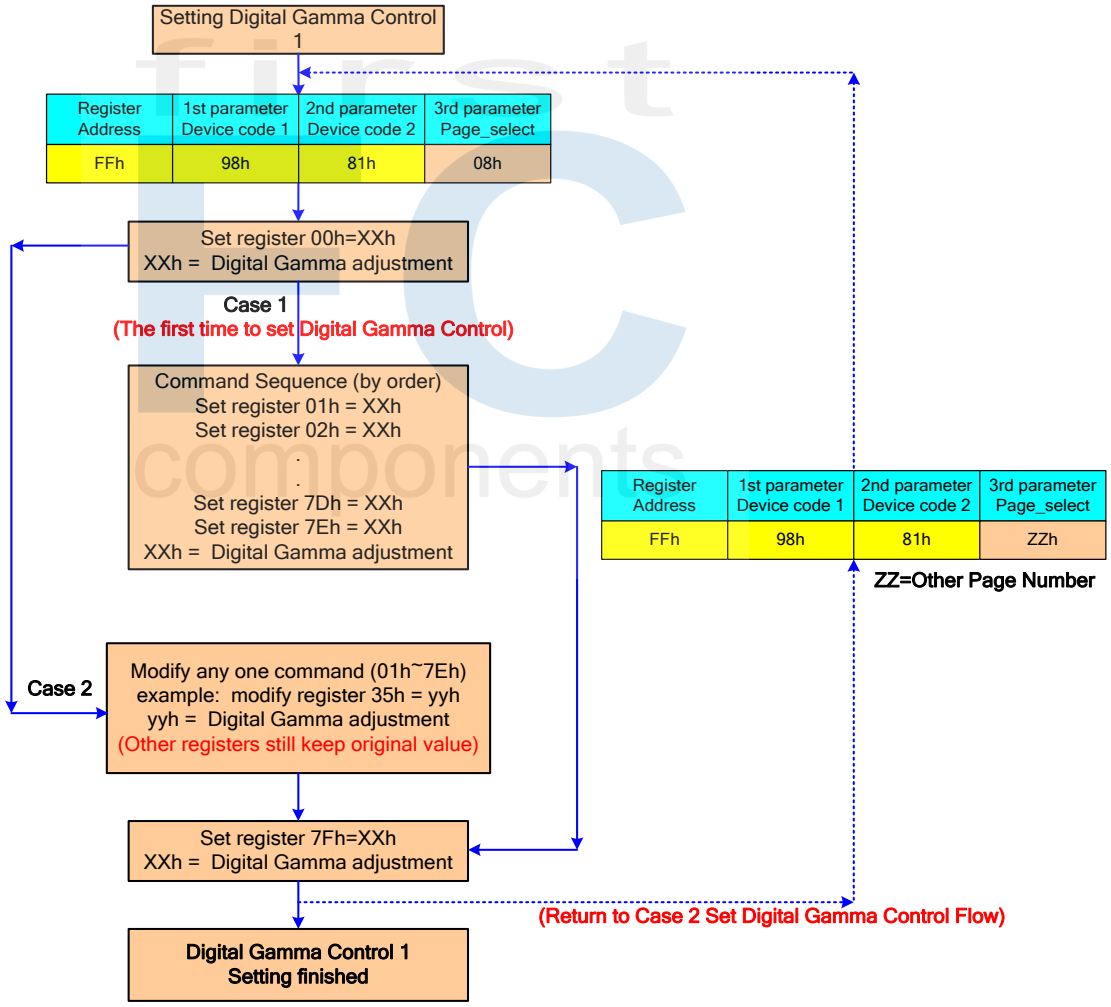
5.11. Page 8 Command Description

5.11.1. Fine Digital Gamma Control 4 (00h~7Fh)

Command Page			Page 8								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	1st	W	GDIN128[7:0]								00h
01h	1st	W	GDIN129[7:0]								00h
02h	1st	W	GDIN130[7:0]								00h
03h	1st	W	GDIN131[7:0]								00h
04h	1st	W	GDIN132[7:0]								00h
05h	1st	W	GDIN133[7:0]								00h
:	1st	W	:								00h
7Ah	1st	W	GDIN250[7:0]								00h
7Bh	1st	W	GDIN251[7:0]								00h
7Ch	1st	W	GDIN252[7:0]								00h
7Dh	1st	W	GDIN253[7:0]								00h
7Eh	1st	W	GDIN254[7:0]								00h
7Fh	1st	W	GDIN255[7:0]								00h

Description

GDINx[7:0]: Digital Gamma Macro-adjustment registers for green gamma curve.



Restriction	None

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<table>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
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</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h_00h_...00h_00h</td></tr>
<tr><td>S/W Reset</td><td>00h_00h_...00h_00h</td></tr>
<tr><td>H/W Reset</td><td>00h_00h_...00h_00h</td></tr>
</table>
</td></tr>
</table>

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5.11.2. EXTC Command Set Enable Register (FFh)

Command Page			Page 8								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
FFh	1st	W	1	0	0	1	1	0	0	0	98h
	2nd	W	1	0	0	0	0	0	0	1	81h
	3rd	W	PAGE[7:0]								08h

Description

PAGE[7:0]: Set the command page.

PAGE[7:0]	Command Page
00h	Page 0
01h	Page 1
02h	Page 2
03h	Page 3
04h	Page 4
05h	Page 5
06h	Page 6
07h	Page 7
08h	Page 8
09h	Page 9
0Ah	Page 10
Others	Reserved

Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available

See section "5.1 Command Flow".

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08h
S/W Reset	08h
H/W Reset	08h

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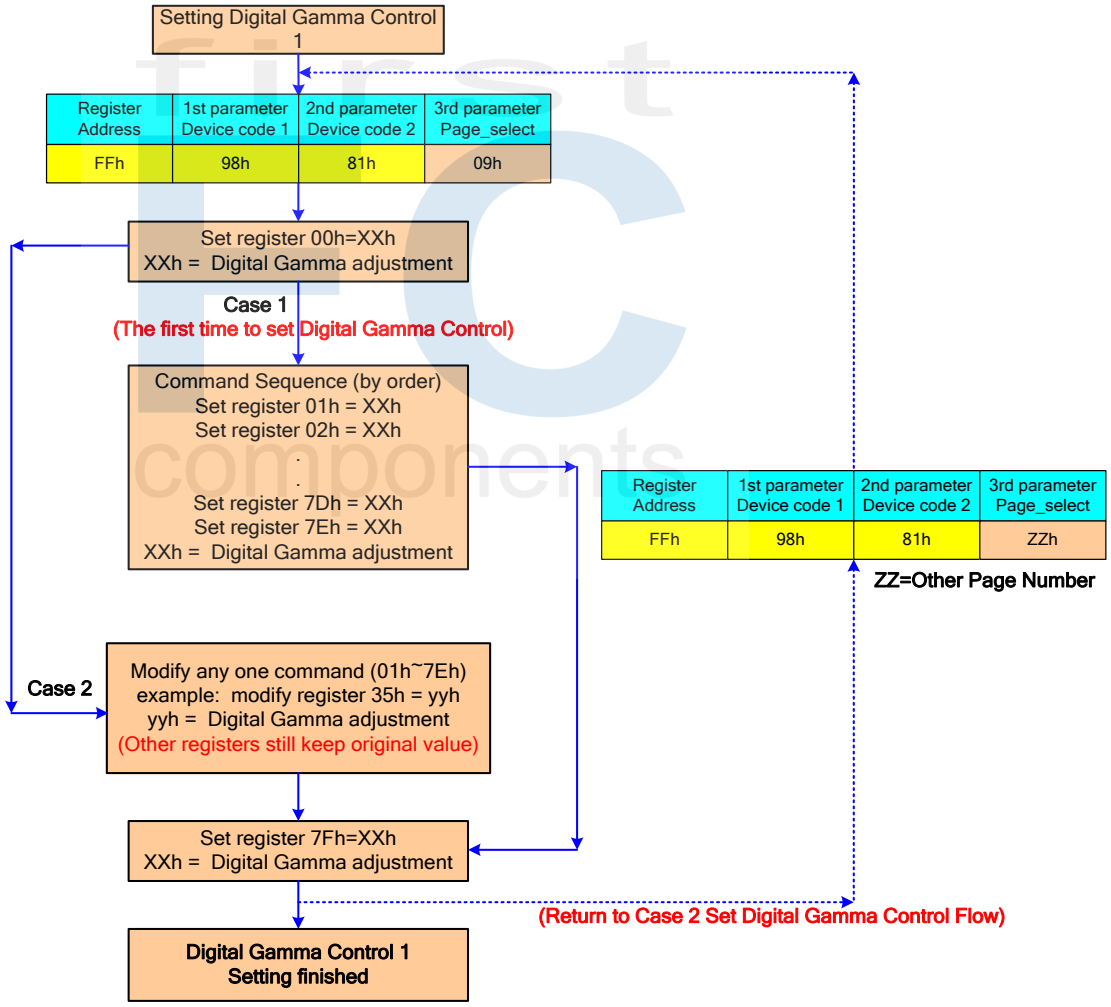
5.12. Page 9 Command Description

5.12.1. Fine Digital Gamma Control 5 (00h~7Fh)

Command Page			Page 9								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	1st	W	BDIN0[7:0]								00h
01h	1st	W	BDIN1[7:0]								00h
02h	1st	W	BDIN2[7:0]								00h
03h	1st	W	BDIN3[7:0]								00h
04h	1st	W	BDIN4[7:0]								00h
05h	1st	W	BDIN5[7:0]								00h
:	1st	W	:								00h
7Ah	1st	W	BDIN122[7:0]								00h
7Bh	1st	W	BDIN123[7:0]								00h
7Ch	1st	W	BDIN124[7:0]								00h
7Dh	1st	W	BDIN125[7:0]								00h
7Eh	1st	W	BDIN126[7:0]								00h
7Fh	1st	W	BDIN127[7:0]								00h

Description

BDINx[7:0]: Digital Gamma Macro-adjustment registers for blue gamma curve.



Restriction	None

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<table>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h_00h_...00h_00h</td></tr>
<tr><td>S/W Reset</td><td>00h_00h_...00h_00h</td></tr>
<tr><td>H/W Reset</td><td>00h_00h_...00h_00h</td></tr>
</table>
</td></tr>
</table>

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5.12.2. EXTC Command Set Enable Register (FFh)

Command Page			Page 9								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
FFh	1st	W	1	0	0	1	1	0	0	0	98h
	2nd	W	1	0	0	0	0	0	0	1	81h
	3rd	W	PAGE[7:0]								09h

Description

PAGE[7:0]: Set the command page.

PAGE[7:0]	Command Page
00h	Page 0
01h	Page 1
02h	Page 2
03h	Page 3
04h	Page 4
05h	Page 5
06h	Page 6
07h	Page 7
08h	Page 8
09h	Page 9
0Ah	Page 10
Others	Reserved

Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available

See section "5.1 Command Flow".

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	09h
S/W Reset	09h
H/W Reset	09h

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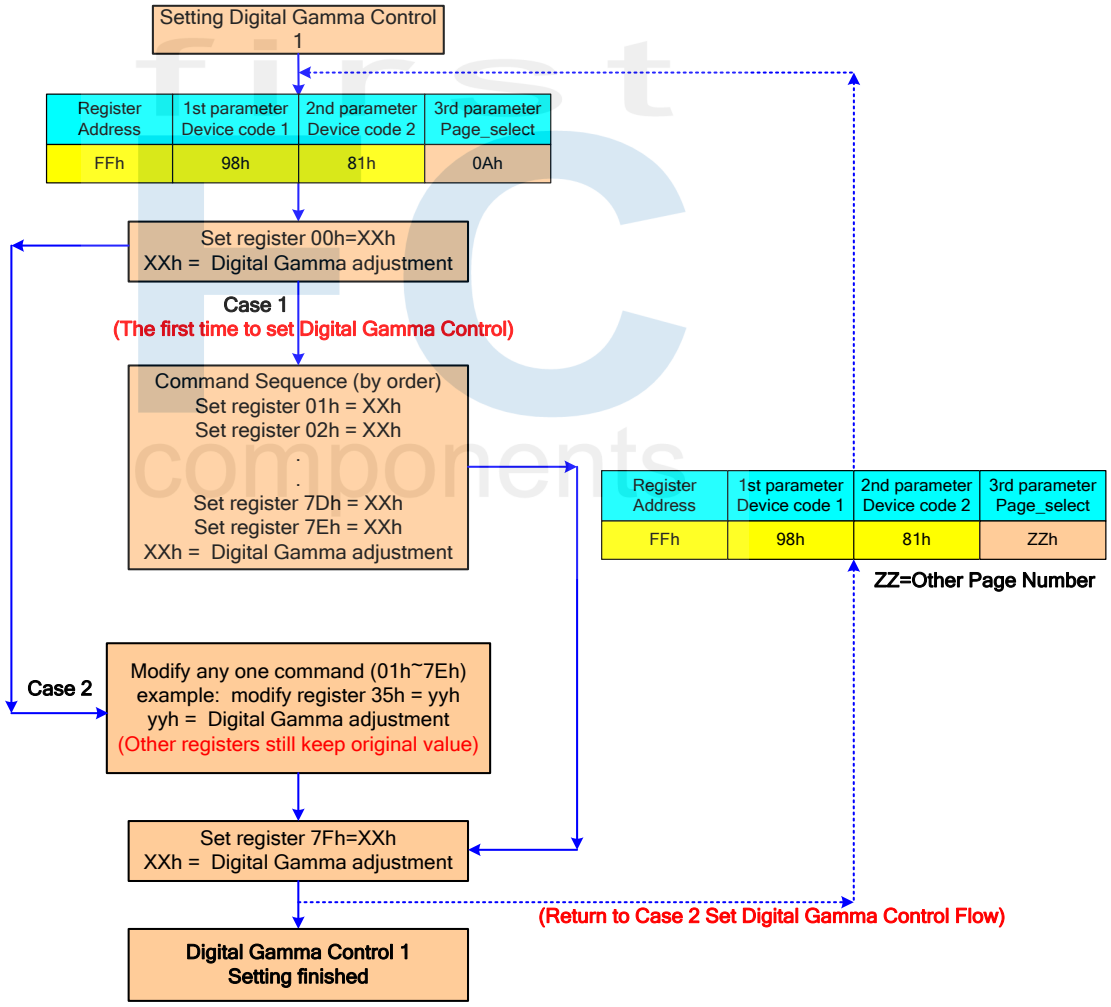
5.13. Page 10 Command Description

5.13.1. Fine Digital Gamma Control 6 (00h~7Fh)

Command Page			Page 10								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	1st	W	BDIN128[7:0]								00h
01h	1st	W	BDIN129[7:0]								00h
02h	1st	W	BDIN130[7:0]								00h
03h	1st	W	BDIN131[7:0]								00h
04h	1st	W	BDIN132[7:0]								00h
05h	1st	W	BDIN133[7:0]								00h
:	1st	W	:								00h
7Ah	1st	W	BDIN250[7:0]								00h
7Bh	1st	W	BDIN251[7:0]								00h
7Ch	1st	W	BDIN252[7:0]								00h
7Dh	1st	W	BDIN253[7:0]								00h
7Eh	1st	W	BDIN254[7:0]								00h
7Fh	1st	W	BDIN255[7:0]								00h

Description

BDINx[7:0]: Digital Gamma Macro-adjustment registers for blue gamma curve.



Restriction	None

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<table>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h_00h_...00h_00h</td></tr>
<tr><td>S/W Reset</td><td>00h_00h_...00h_00h</td></tr>
<tr><td>H/W Reset</td><td>00h_00h_...00h_00h</td></tr>
</table>
</td></tr>
</table>

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5.13.2. EXTC Command Set Enable Register (FFh)

Command Page			Page 10								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
FFh	1st	W	1	0	0	1	1	0	0	0	98h
	2nd	W	1	0	0	0	0	0	0	1	81h
	3rd	W	PAGE[7:0]								0Ah

Description

PAGE[7:0]: Set the command page.

PAGE[7:0]	Command Page
00h	Page 0
01h	Page 1
02h	Page 2
03h	Page 3
04h	Page 4
05h	Page 5
06h	Page 6
07h	Page 7
08h	Page 8
09h	Page 9
0Ah	Page 10
Others	Reserved

Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available

See section "5.1 Command Flow".

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0Ah
S/W Reset	0Ah
H/W Reset	0Ah

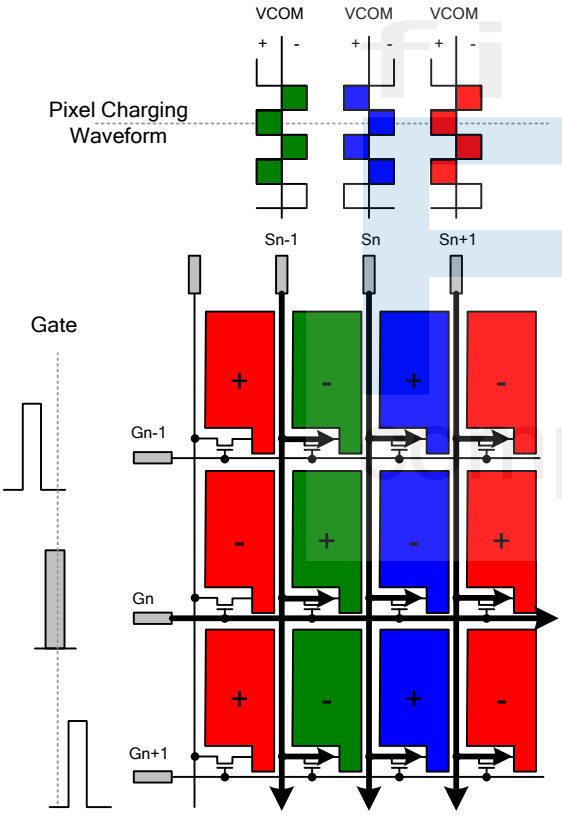
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6. Source Driver

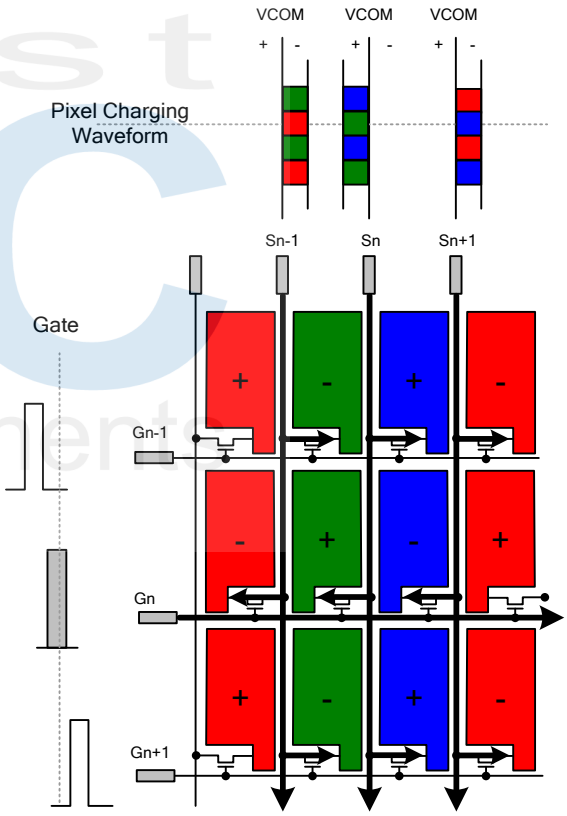
The source driver uses 2402 channels (S1~S2400 and SDUM[2:1] channels) for the Zig-zag function used for driving the source line of the TFT LCD panel. The source driver converts the digital data into the analog voltage and generates corresponding gray scale voltage output, enabling up to 16.7M colors to be displayed simultaneously. The output circuit of this source driver incorporates an operational amplifier, so that a positive and a negative voltage can be alternately outputted from each channel.

6.1. Zig-zag Inversion

Zig-zag Inversion is used to reduce the power consumption. The Zig-zag inversion decreases the switching frequency of the source related to the magnitude of power consumption. This method will have an addendum data line, SDUM.



1-Dot Inversion Driving

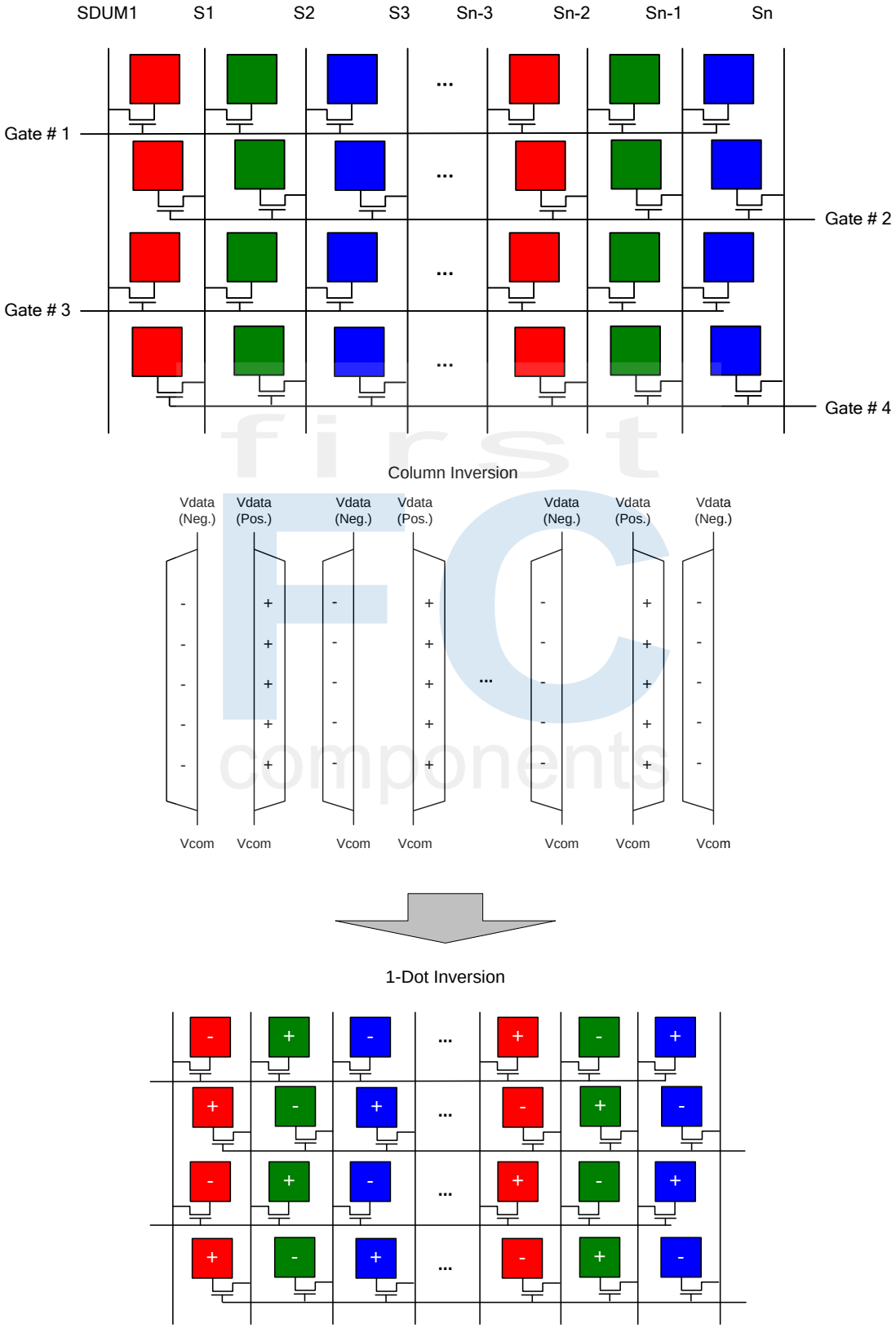


Vertical Bi-Color driving

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6.2. Zig-zag Inversion Concept

The Zig-zag method uses the same polarity of data line of the column inversion to show the 1-dot inversion.



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6.3. Zig-zag Inversion Source Output Method

The driving panel display method adds one sub-pixel at the Gate_Even to shift the data output.

(At the Gate_Even line, an additional data line is utilized.)

Red Pattern

	SDUM1	S1	S2	S3	S4	S5	Sn-5	Sn-4	Sn-3	Sn-2	Sn-1	Sn
Gate_Odd	R1	G1	B1	R2	G2	B2	Gx-1	Bx-1	Rx	Gx	Bx	
Gate_Even		R1	G1	B1	R2	G2	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx
Gate_Odd	R1	G1	B1	R2	G2	B2	Gx-1	Bx-1	Rx	Gx	Bx	
Gate_Even		R1	G1	B1	R2	G2	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx
Gate_Odd	R1	G1	B1	R2	G2	B2	Gx-1	Bx-1	Rx	Gx	Bx	
Gate_Even		R1	G1	B1	R2	G2	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx

Green Pattern

	SDUM1	S1	S2	S3	S4	S5	Sn-5	Sn-4	Sn-3	Sn-2	Sn-1	Sn
Gate_Odd	R1	G1	B1	R2	G2	B2	Gx-1	Bx-1	Rx	Gx	Bx	
Gate_Even		R1	G1	B1	R2	G2	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx
Gate_Odd	R1	G1	B1	R2	G2	B2	Gx-1	Bx-1	Rx	Gx	Bx	
Gate_Even		R1	G1	B1	R2	G2	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx
Gate_Odd	R1	G1	B1	R2	G2	B2	Gx-1	Bx-1	Rx	Gx	Bx	
Gate_Even		R1	G1	B1	R2	G2	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx

Blue Pattern

	SDUM1	S1	S2	S3	S4	S5	Sn-5	Sn-4	Sn-3	Sn-2	Sn-1	Sn
Gate_Odd	R1	G1	B1	R2	G2	B2	Gx-1	Bx-1	Rx	Gx	Bx	
Gate_Even		R1	G1	B1	R2	G2	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx
Gate_Odd	R1	G1	B1	R2	G2	B2	Gx-1	Bx-1	Rx	Gx	Bx	
Gate_Even		R1	G1	B1	R2	G2	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx
Gate_Odd	R1	G1	B1	R2	G2	B2	Gx-1	Bx-1	Rx	Gx	Bx	
Gate_Even		R1	G1	B1	R2	G2	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx

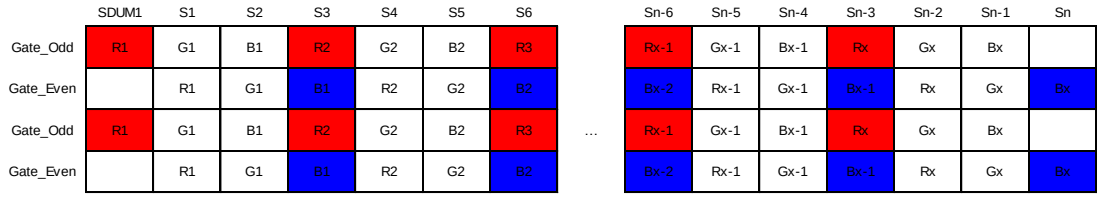
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6.4. Zig-zag Inversion RED Data Display

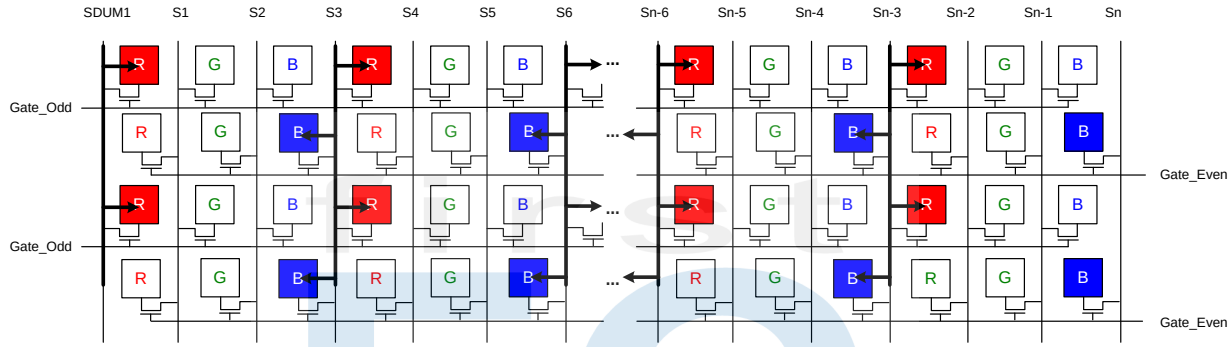
The figure below illustrates the Zig-zag inversion panel driving method for Red data input.

When driving a Red pattern, the Red and Blue sub-pixels will light up line by line according to the data signal input.

Source Output

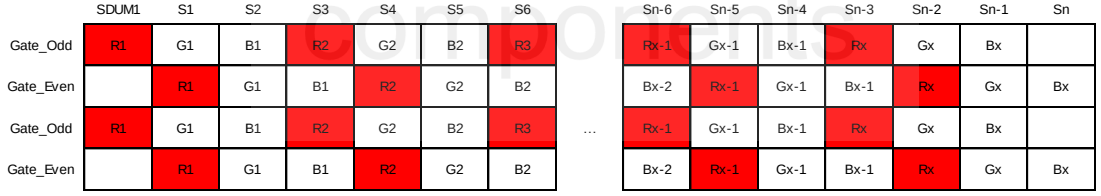


Panel Driving

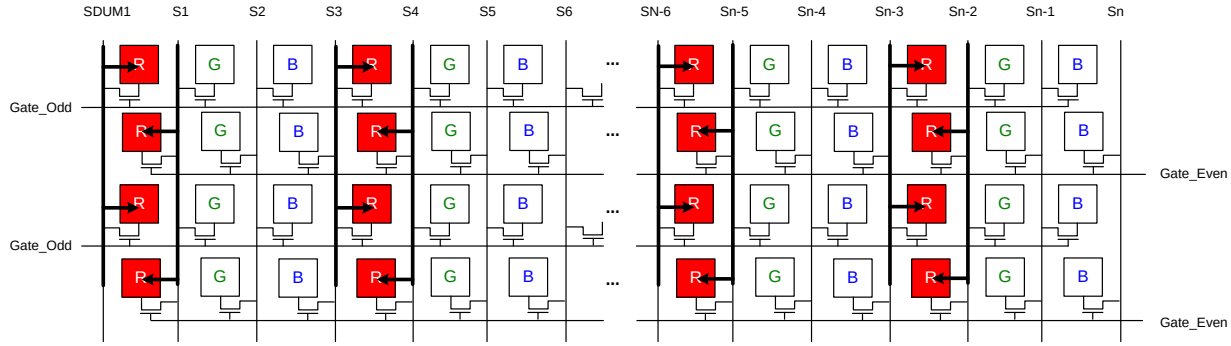


The figure below is the Zig-zag inversion panel driving method. The panel will be driven by the Red data input of the Gate_Odd and the Green data input of the Gate_Even.

Source Output



Panel Driving



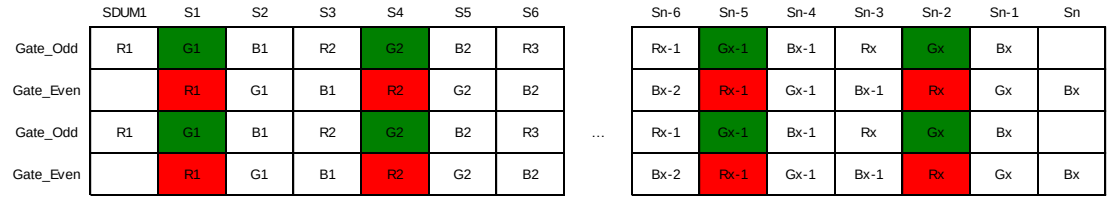
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6.5. Zig-zag Inversion GREEN Data Display

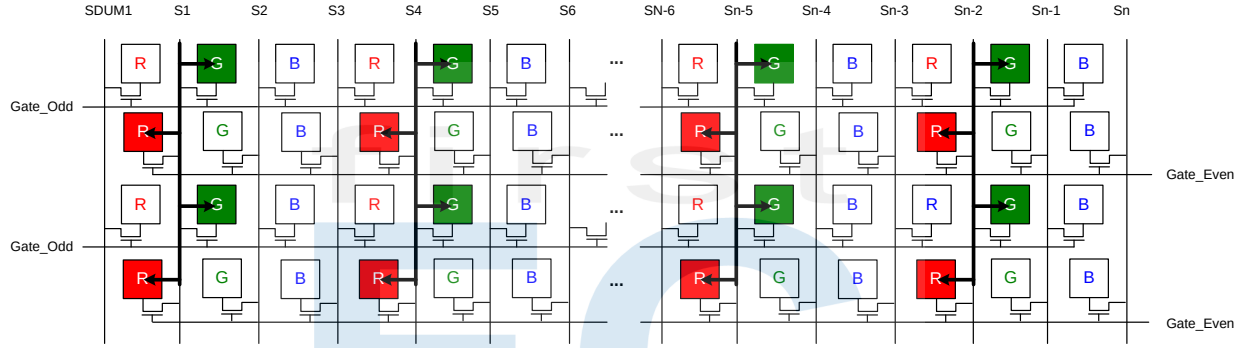
The figure below illustrates the Zig-zag inversion panel driving method for Green data input.

When driving a Green pattern, the Green and Red sub-pixels will light up line by line according to the data signal input.

Source Output

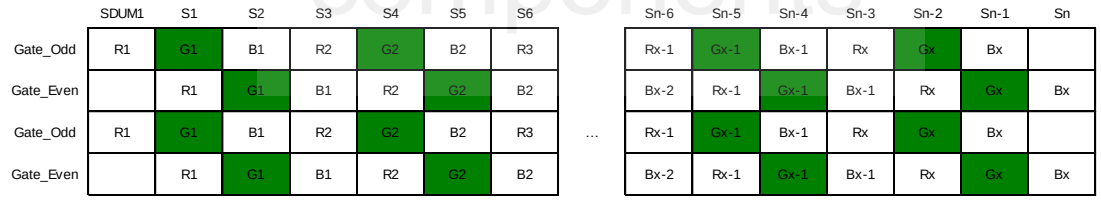


Panel Driving

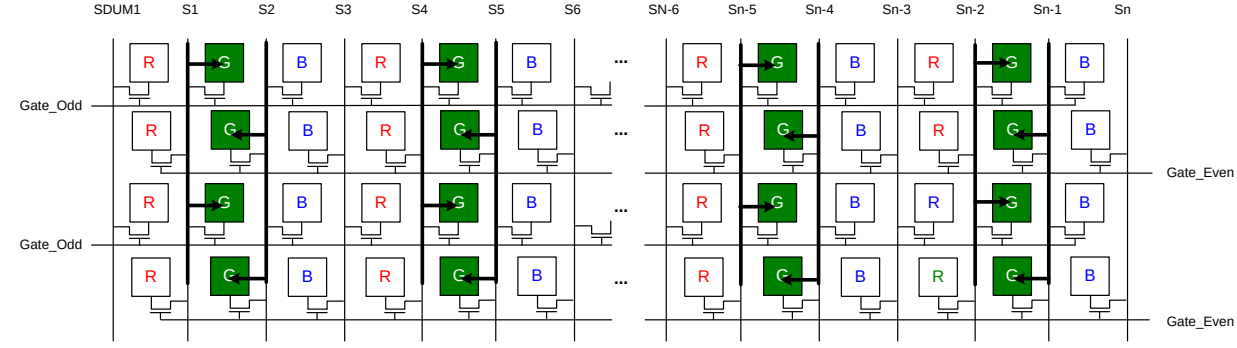


The figure below is the Zig-zag inversion panel driving method. The panel will be driven by the Green data input of the Gate_Odd and the Blue data input of the Gate_Even.

Source Output



Panel Driving



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6.6. Zig-zag Inversion BLUE Data Display

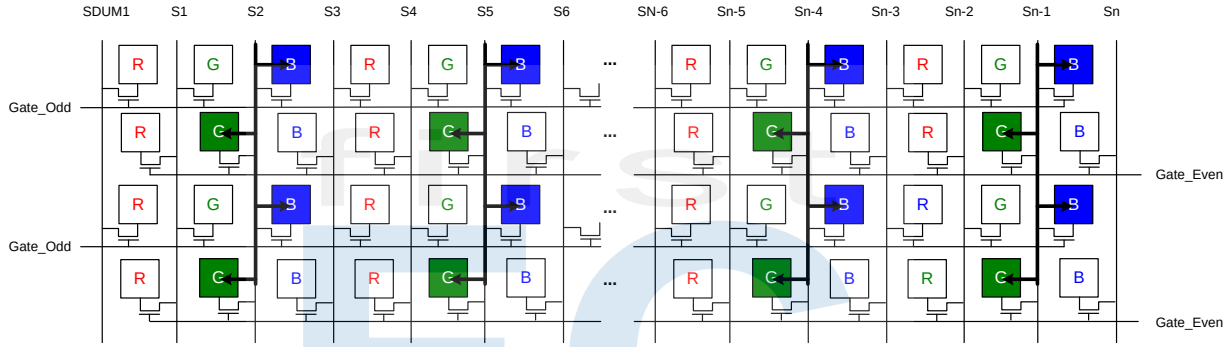
The figure below illustrates the Zig-zag inversion panel driving method for Blue data input.

When driving a Blue pattern, the Blue and Green sub-pixels will light up line by line according to the data signal input.

Source Output

	SDUM1	S1	S2	S3	S4	S5	S6		Sn-6	Sn-5	Sn-4	Sn-3	Sn-2	Sn-1	Sn
Gate_Odd	R1	G1	B1	R2	G2	B2	R3		Rx-1	Gx-1	Bx-1	Rx	Gx	Bx	
Gate_Even		R1	G1	B1	R2	G2	B2		Bx-2	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx
Gate_Odd	R1	G1	B1	R2	G2	B2	R3	...	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx	
Gate_Even		R1	G1	B1	R2	G2	B2		Bx-2	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx

Panel Driving

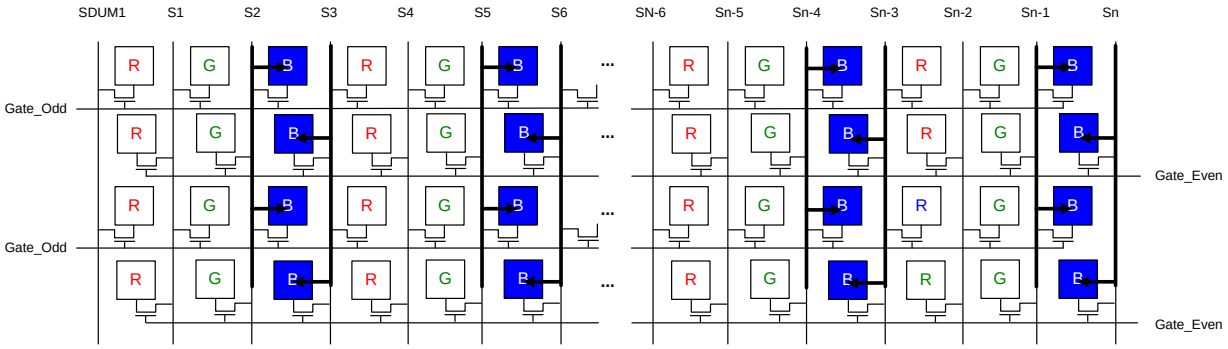


The figure below is the Zig-zag inversion panel driving method. The panel will be driven by the Blue data input of the Gate_Odd and the Red data input of the Gate_Even.

Source Output

	SDUM1	S1	S2	S3	S4	S5	S6		Sn-6	Sn-5	Sn-4	Sn-3	Sn-2	Sn-1	Sn
Gate_Odd	R1	G1	B1	R2	G2	B2	R3		Rx-1	Gx-1	Bx-1	Rx	Gx	Bx	
Gate_Even		R1	G1	B1	R2	G2	B2		Bx-2	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx
Gate_Odd	R1	G1	B1	R2	G2	B2	R3	...	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx	
Gate_Even		R1	G1	B1	R2	G2	B2		Bx-2	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx

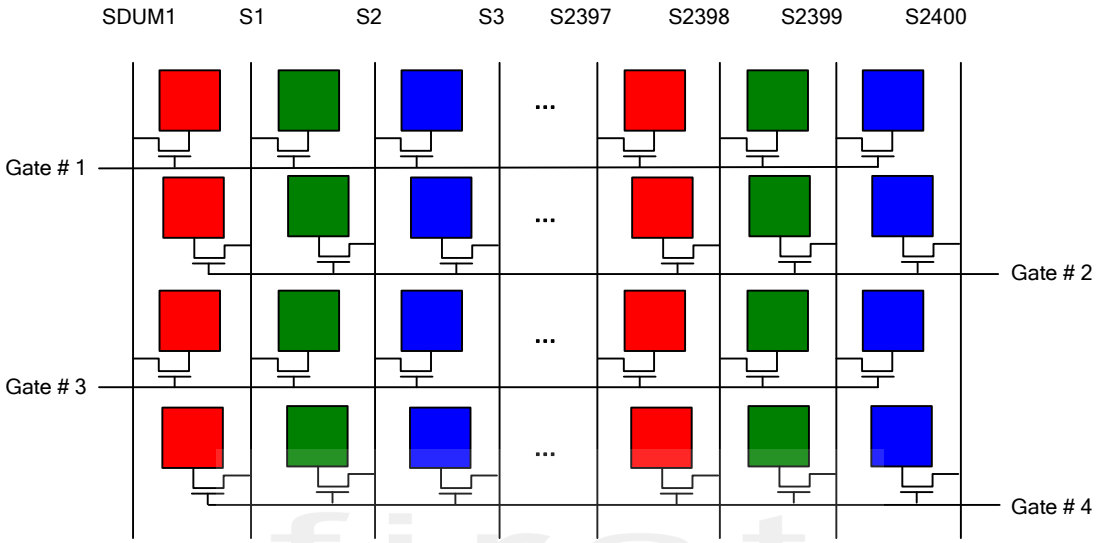
Panel Driving



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6.7. Different Zig-zag Type Panel

Zig-zag Type 1 (DINV[3:0] = 9h)

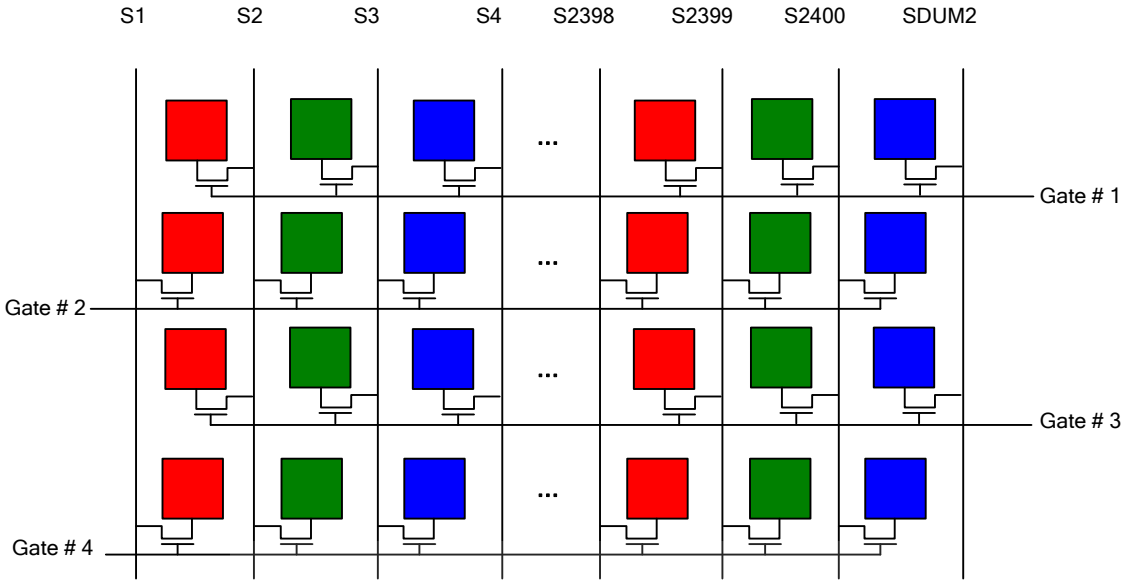


Zig-zag Type 2 (DINV[3:0] = Ah)

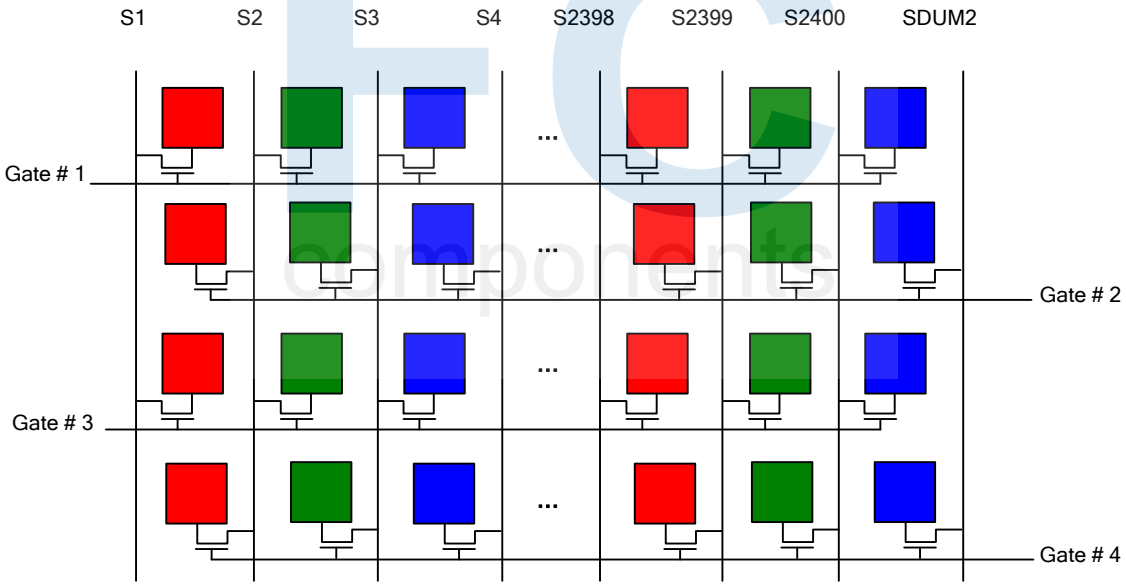


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Zig-zag Type 3 (DINV[3:0] = Bh)



Zig-zag Type 4 (DINV[3:0] = Ch)



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7. Enter/Exit Idle Mode Flow

7.1. Enter/Exit Idle Mode Flow

Input data format in Idle Mode shall use uncompressed 24 bit/pixel Writing and full-frame pixel data are carried in command mode using Memory Write Start and Memory Write Continue commands.

Following figure describes sequence to enter Idle Mode .

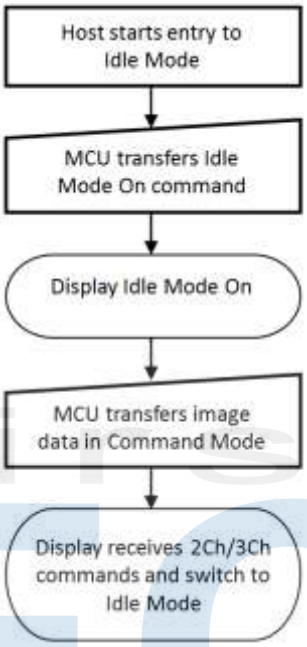


Figure 92: Enter Idle Mode Flow

Following figure describes sequence to exit Idle Mode and switch back to Video Mode operation.

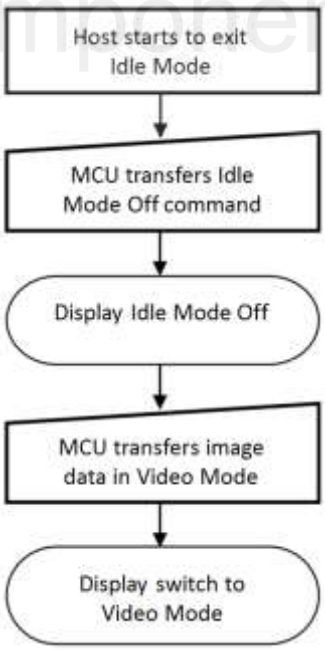


Figure 93: Exit Idle Mode Flow

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7.2. Enter/Exit Idle Mode sequence

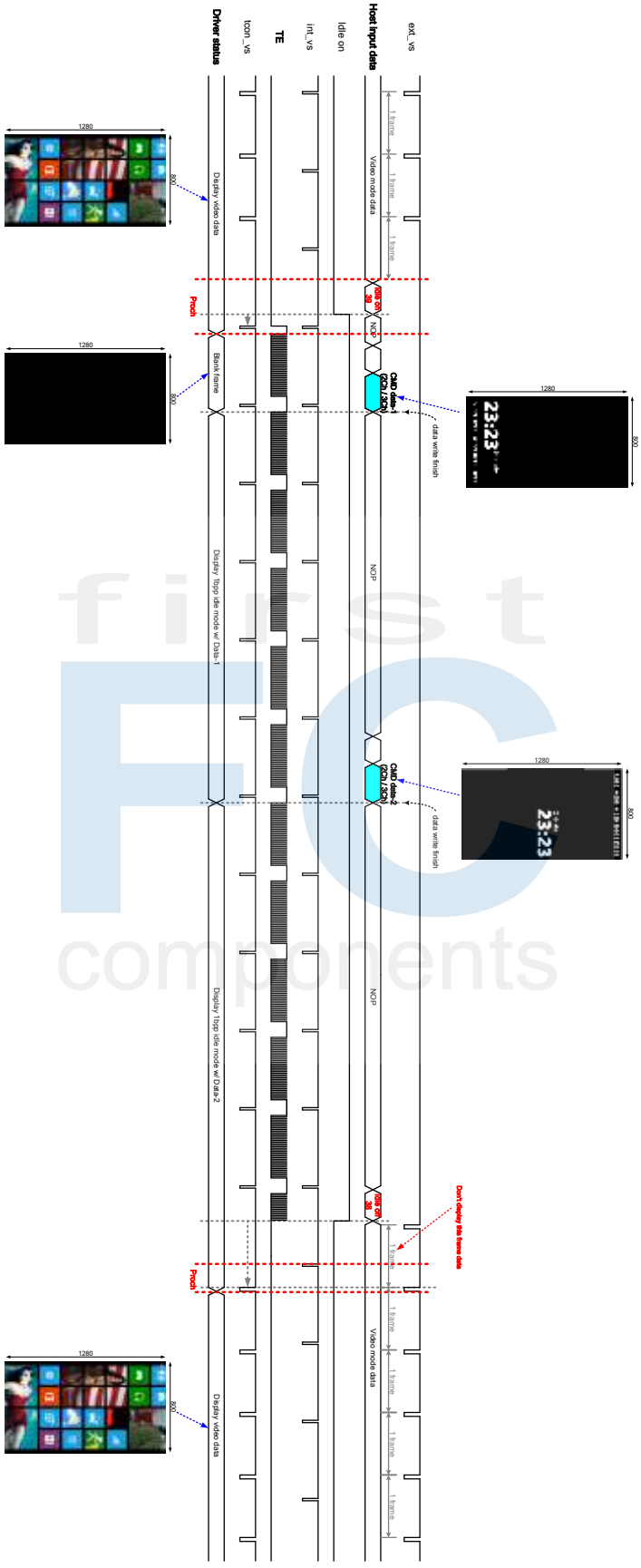


Figure 94: Enter/Exit Idle Mode Sequence

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8. BIST Mode Function

8.1. BIST Mode Pattern

Table 33: BIST Mode Pattern

FRM_PT[0] White	FRM_PT[1] Black	FRM_PT[2] Red	FRM_PT[3] Green
FRM_PT[4] Blue	FRM_PT[5] Gray128	FRM_PT[6] Gray127	FRM_PT[7] V-Color bar

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9. Content Adaptive Brightness Control (CABC) Function

The CABC, a dynamic backlight control function, drastically reduces the power consumption of the luminance source. The ILI9881C-0D will refer the gray scale content of the display image to output in PWM waveform then to the LED driver for backlight brightness control. The content of gray scale can be increased while simultaneously lowering the brightness of the backlight to achieve the same perceived brightness. The adjusted gray level scale and the power consumption reduction depend on the content of the image.

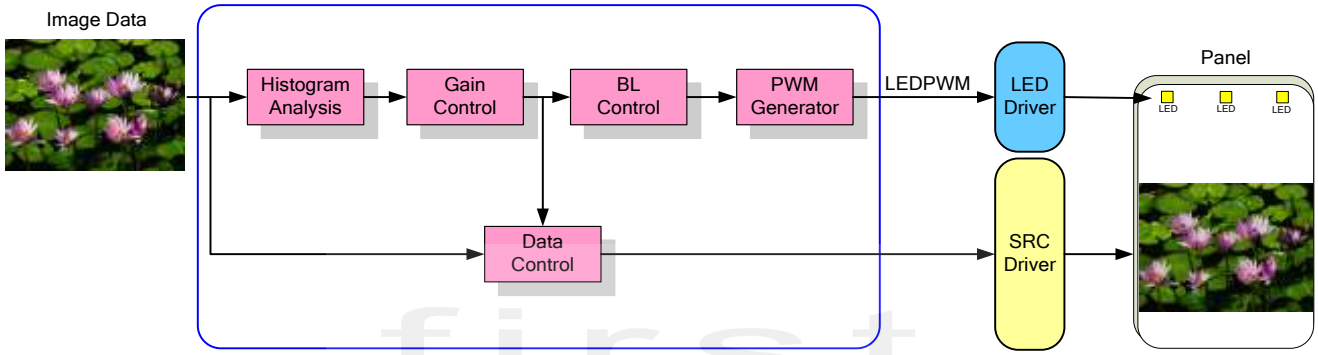


Figure 95: CABC Block Diagram

The ILI9881C-0D can calculate the backlight brightness level and send a PWM_OUT pulse to the LED driver via LEDPWM pin for backlight brightness control purposes. The PWM frequency can be adjusted by PWM_DIV parameters, and the calculating equation is shown below:

$$f_{LEDPWM} = \frac{32\ MHz}{(\text{PWM_DIV}[7:0] + 1) \times PWM_DUTY_PRECISION}$$

Figure 96 is the basic timing diagram which is applied from the ILI9881C-0D in order to control the LED driver.

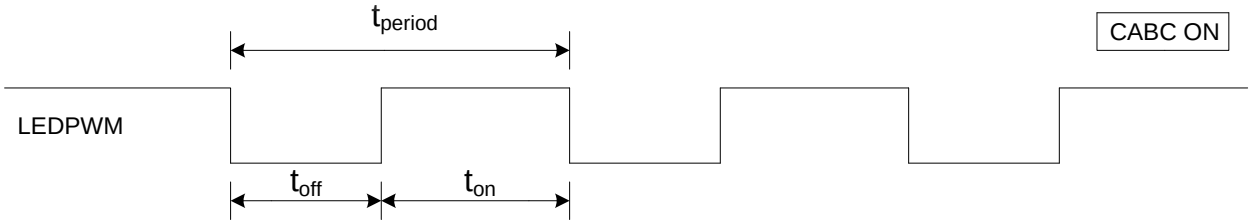


Figure 96: PWM OUT On/Off Period

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10. Color Enhancement Function

10.1. Saturation Enhancement

The ILI9881C-0D provides the saturation enhancement to make the image content more vivid. The main concept in this feature is to enhance the color information on HSL domain, which includes the saturation information of each different color, show as Figure 97.



Figure 97: Saturation Enhancement : HSL model

In Figure 98, there is an example for saturation enhancement. Different enhancement levels being applied in this example.



(a) **(b)** **(c)** **(d)**

Figure 98: Saturation Enhancement Image (a) Original, (b) Low Level, (c) Medium Level, (d) High Level.

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10.2. Contrast Enhancement

The contrast between the dark and light, indicate the clarity of the image content. In this design, it provides contrast enhancement to increase the difference between dark and light to achieve the high contrast image. The user can select the enhancement level by setting command, the example shows below.



(a) (b)

Figure 99: Contrast Enhancement Image (a) Original, (b) After enhancement

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10.3. Sharpness Enhancement

Sharpness enhancement is provided to enhance the image visibility. Unlike contrast enhancement, sharpness enhancement is to strengthen the object's edge to make the object more clearly. The user can select the enhancement level by setting command, the example shows below.



(a) **(b)**

Figure 100: Sharpness Enhancement Image (a) Original, (b) After enhancement

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10.4. Sunlight Readability

The sunlight readability is in order to achieve high visibility in daylight or other bright light condition. Figure 101 shows the main concept of the influence of ambient light to the LCD displayer and the solution in the high ambient light condition. In this design, it changes the image content to achieve the high visibility in the ambient light condition as shows in Figure 101(b).

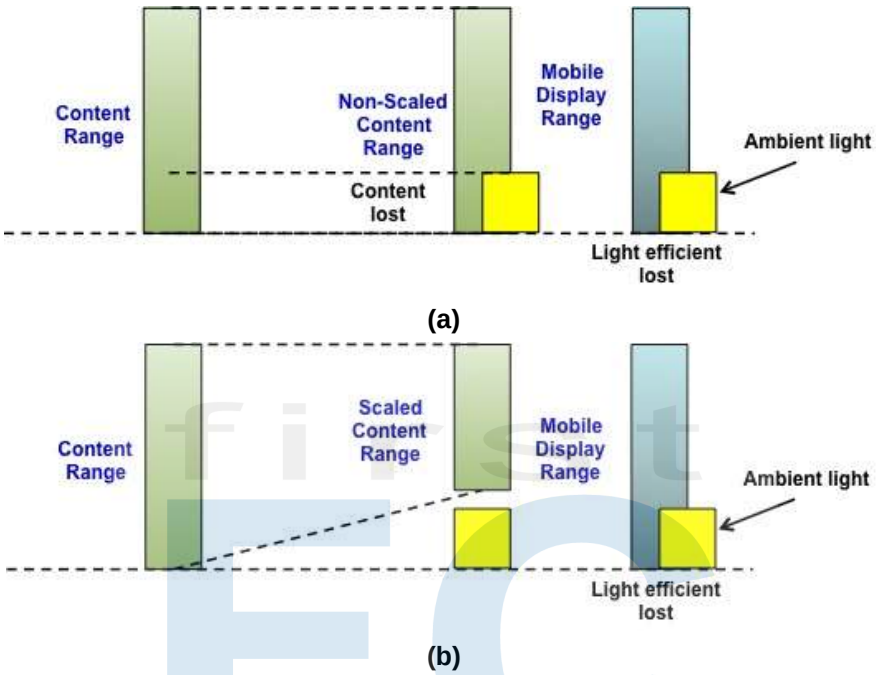


Figure 101: Sunlight Readability Concept (a) Backlight efficiency is consumed by ambient light, (b)Enhance the image content to avoid the influence.

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11. Sleep Out Command and Self-Diagnostic Functions

11.1. Register Loading Detection

Sleep Out command (See Sleep Out (11h)) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller works properly.

The display controller will compare factory values of the EEPROM and register values of the display controller (1st step: compare register and EEPROM values; 2nd step: load EEPROM value to the register). If those two values (EEPROM and register values) are the same, a bit is inverted (= increased by 1), which is defined in command Read Display Self-Diagnostic Result (0Fh) (= RDDSDR) (The used bit of this command is D7). If those values are not the same, this bit (D7) is not inverted (= not increased by 1). The flow chart for this internal function is as follows:

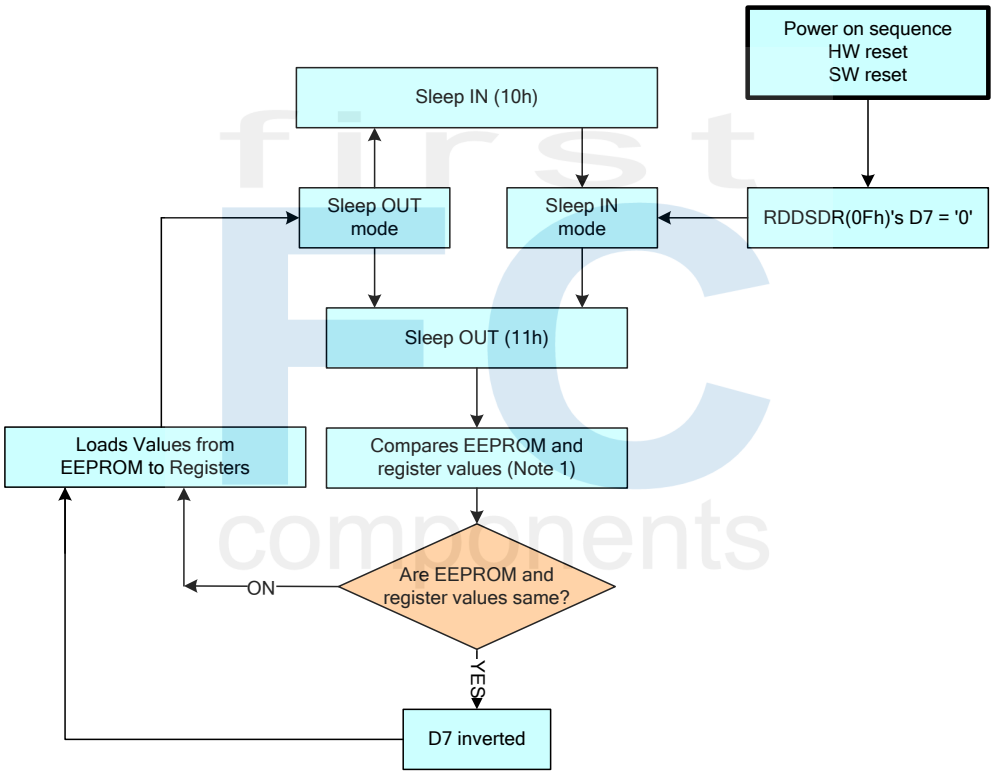


Figure 102: Register Loading Detection

Notes: *If the EEPROM and loaded register values are not compared, then they can be changed by 00h to AFh and DAh to DDh commands.*

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11.2. Functionality Detection

The Sleep Out command (See Sleep Out (11h)) is a trigger for an internal function of the display module. It indicates if the display module is still running and meets functionality requirements. The internal function (the display controller) is compared to check if the display module still meets functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirements are met, a bit is inverted (= increased by 1), defined in the command Read Display Self-Diagnostic Result (0Fh) (RDDSDR) (The used bit of this command is D6). If functionality requirement is not the same, this bit (D6) is not inverted (= not increased by 1). The flow chart for this internal function is as follows:

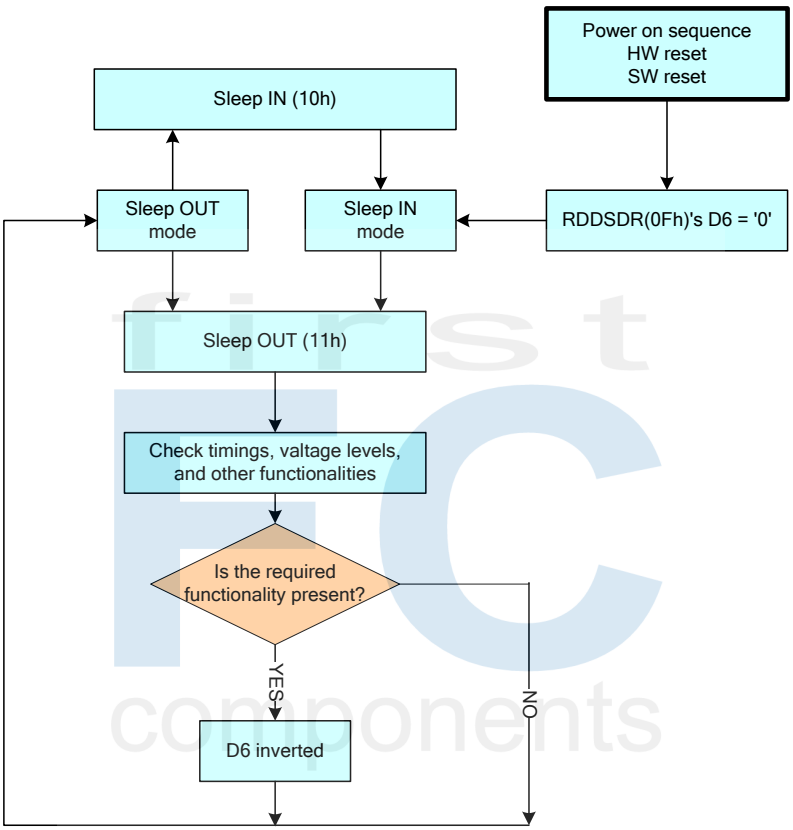


Figure 103: Functionality Detection

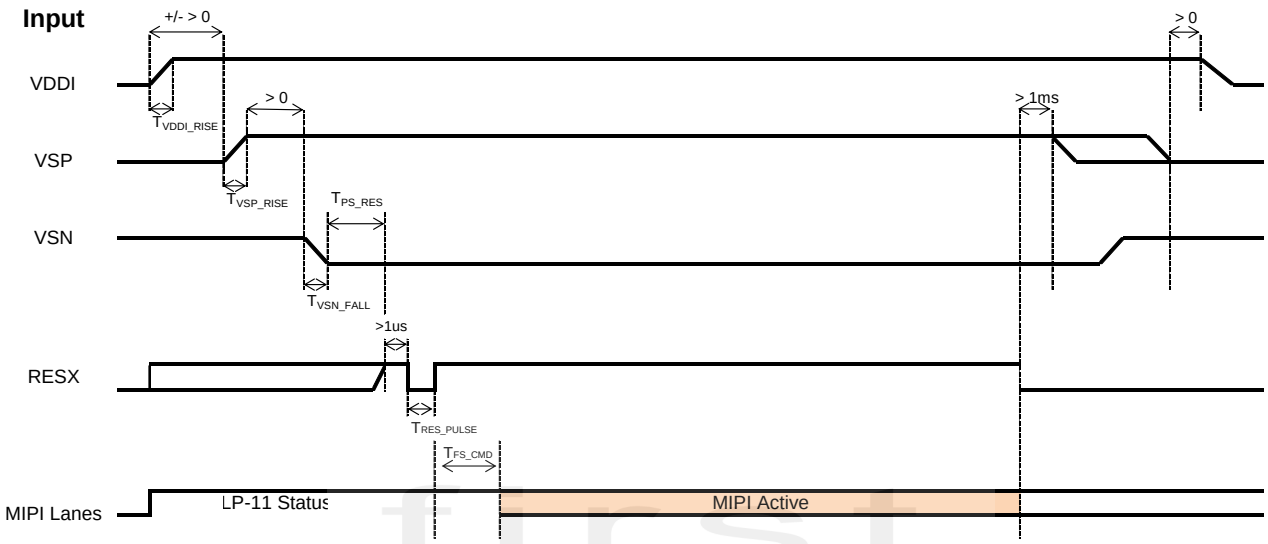
Notes: *When changing from the Sleep In mode to Sleep Out mode, 120msec are needed after the Sleep Out command before it is able to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there will be 5msec delay for the D6's value to be valid when the Sleep Out command is sent in the Sleep Out mode.*

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12. Power on/off Sequence

12.1. Power on/off sequence

12.1.1. Power Mode 2A



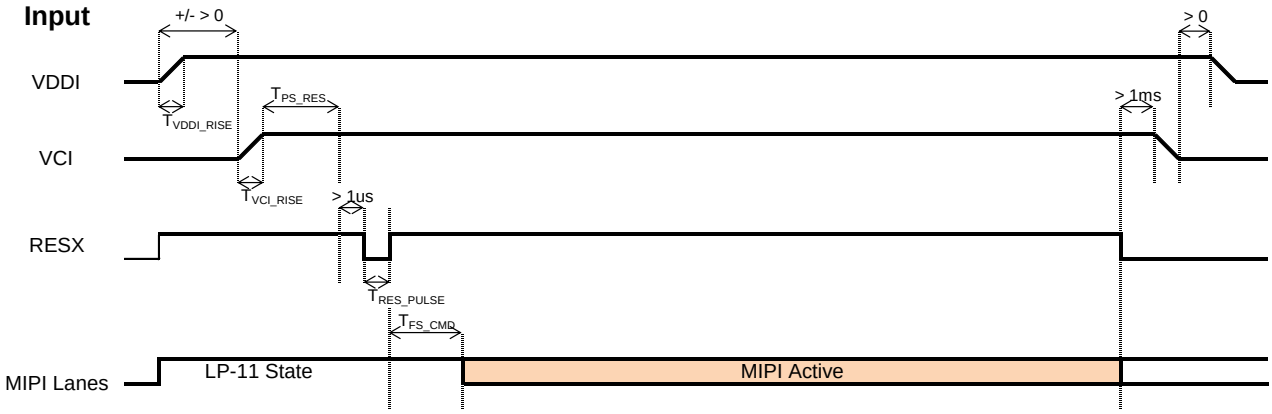
Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VSP_RISE}	VSP Rise time	130	-	-	us
T_{VSN_FALL}	VSN Fall time	200	-	-	us
T_{PS_RES}	VDDI/VSP on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

Figure 104: Power on/off sequence with Power Mode 2A

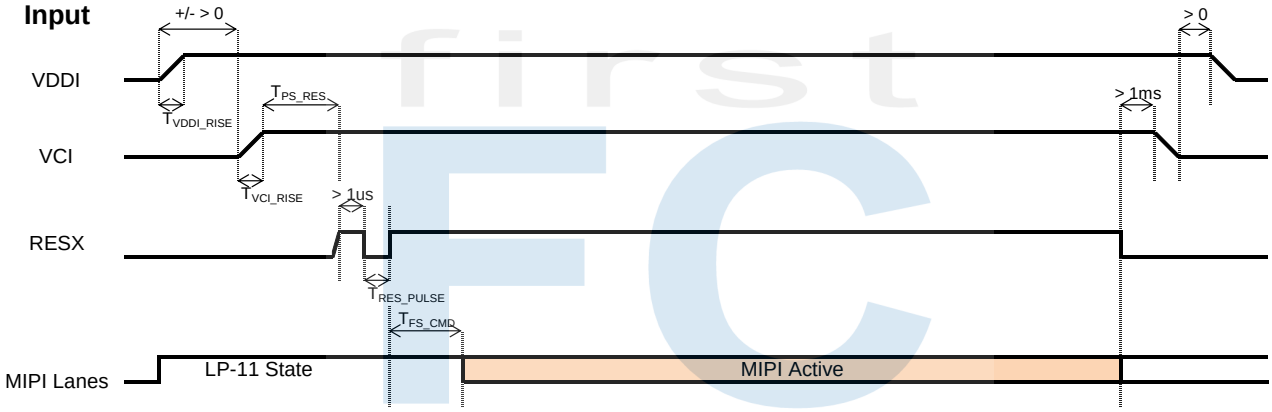
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12.1.2. Power Mode 3

Case A:



Case B:

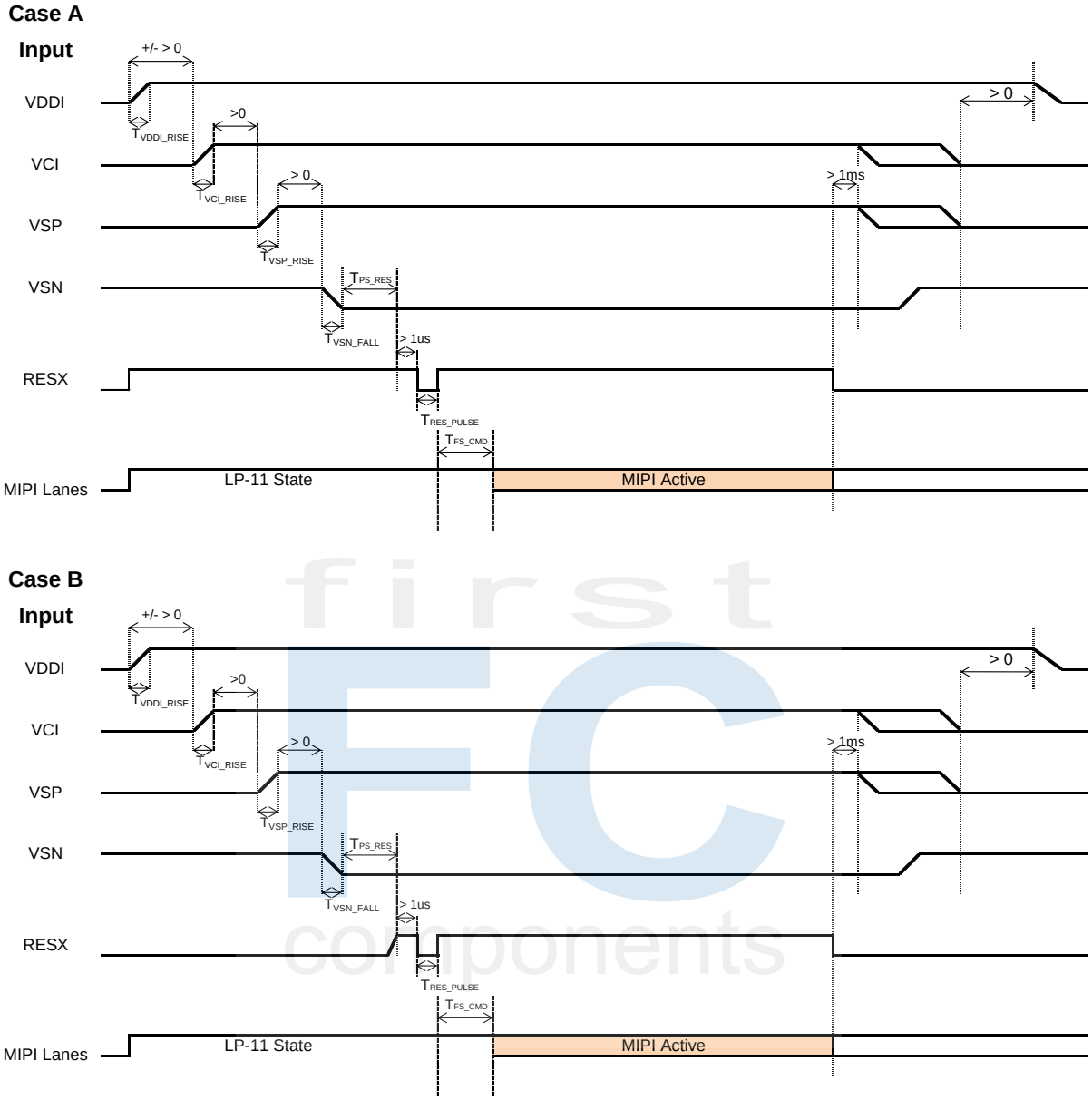


Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VCI_RISE}	Case A: VCI Rise time	130	-	-	us
	Case B: VCI Rise time	40			
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

Figure 105: Power on/off sequence with Power Mode 3

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12.1.3. Power Mode 4



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VCI_RISE}	Case A: VCI Rise time	130	-	-	us
	Case B: VCI Rise time	40			
T_{VSP_RISE}	VSP Rise time	130	-	-	us
T_{VSN_FALL}	VSN Fall time	200	-	-	us
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

Figure 106: Power on/off sequence with Power Mode 4

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12.2. Uncontrolled Power Off

The uncontrolled power off means a situation when a battery is removed without the controlled power off sequence. There will not be any damages for the display module, or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off event, the ILI9881C-0D will force the display to become blank and will not have any abnormal visible effects within 1 second on the display and remains blank until the Power On Sequence powers it up.

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13. Power Level Definition

13.1. Power Levels

4 level modes are defined in order from Maximum to Minimum Power consumption:

1. Normal Mode On (full display), Sleep Out, Idle Mode Off.
   In this mode, the display is able to show a maximum of 16.7M colors.
2. Normal Mode On (full display), Sleep Out, Idle Mode On.
   In this mode, the display is able to show a maximum of 2 colors.
3. Sleep In Mode.
   In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped.
4. Power Off Mode.
   In this mode, all input powers are removed.

Transition between modes 1-3 is controllable by MCU commands. Mode 4 is entered only when both Power supplies are removed.

13.2. Power Flow Chart

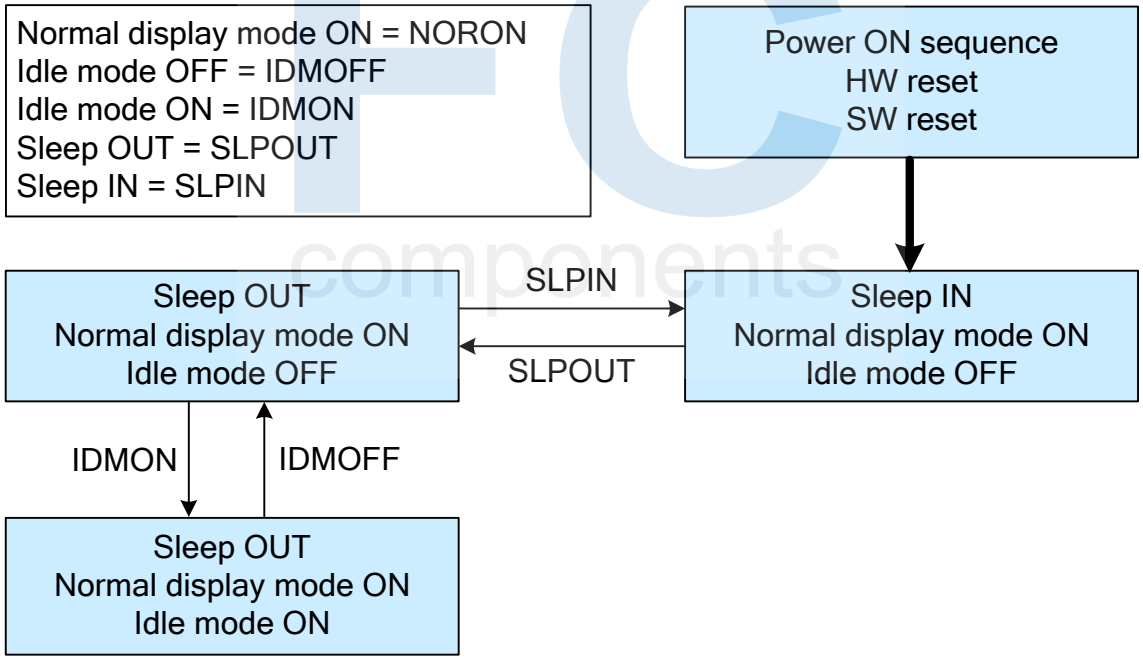


Figure 1075: Power Mode Flow Chart

Notes:

1. *There is not any abnormal visual effect when one power mode changes to another power mode.*
2. *There is not any limitation, which is not specified by User, when one power mode changes to another power mode.*

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14. Characteristics of I/O

14.1. Output or Bi-directional (I/O) Pins

Table 34: Characteristics of Output or Bi-directional (I/O) Pins

Pin/Line	After Power ON	After Hardware Reset	After Software Reset
D0P	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
D0N	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
VS	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
HS	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
LEDPWM	Low	Low	Low
TE	Low	Low	Low

Note: *There will be no output from D0P, D0N, VS, HS, LEDPWM and TE during Power ON/OFF sequence, hardware reset, and software reset.*

14.2. Input Pins

Table 35: Input Pins

Pin/Line	During Power ON Process	After Power ON	After Hardware Reset	After Software Reset	During Power OFF Process
RESX	See chapter 12	Input valid	Input valid	Input valid	See chapter 12
IM[2:0]	Input invalid	Input valid	Input valid	Input valid	Input invalid
LANSEL	Input invalid	Input valid	Input valid	Input valid	Input invalid
RS[1:0]	Input invalid	Input valid	Input valid	Input valid	Input invalid
BOOSTM[2:0]	Input invalid	Input valid	Input valid	Input valid	Input invalid
CLKP	Input invalid	Input valid	Input valid	Input valid	Input invalid
CLKN	Input invalid	Input valid	Input valid	Input valid	Input invalid
D0P	Input invalid	Input valid	Input valid	Input valid	Input invalid
D0N	Input invalid	Input valid	Input valid	Input valid	Input invalid
D1P	Input invalid	Input valid	Input valid	Input valid	Input invalid
D1N	Input invalid	Input valid	Input valid	Input valid	Input invalid
D2P	Input invalid	Input valid	Input valid	Input valid	Input invalid
D2N	Input invalid	Input valid	Input valid	Input valid	Input invalid
D3P	Input invalid	Input valid	Input valid	Input valid	Input invalid
D3N	Input invalid	Input valid	Input valid	Input valid	Input invalid

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15. NV Memory Programming Flow

15.1. External MTP_PWR Programming Flow

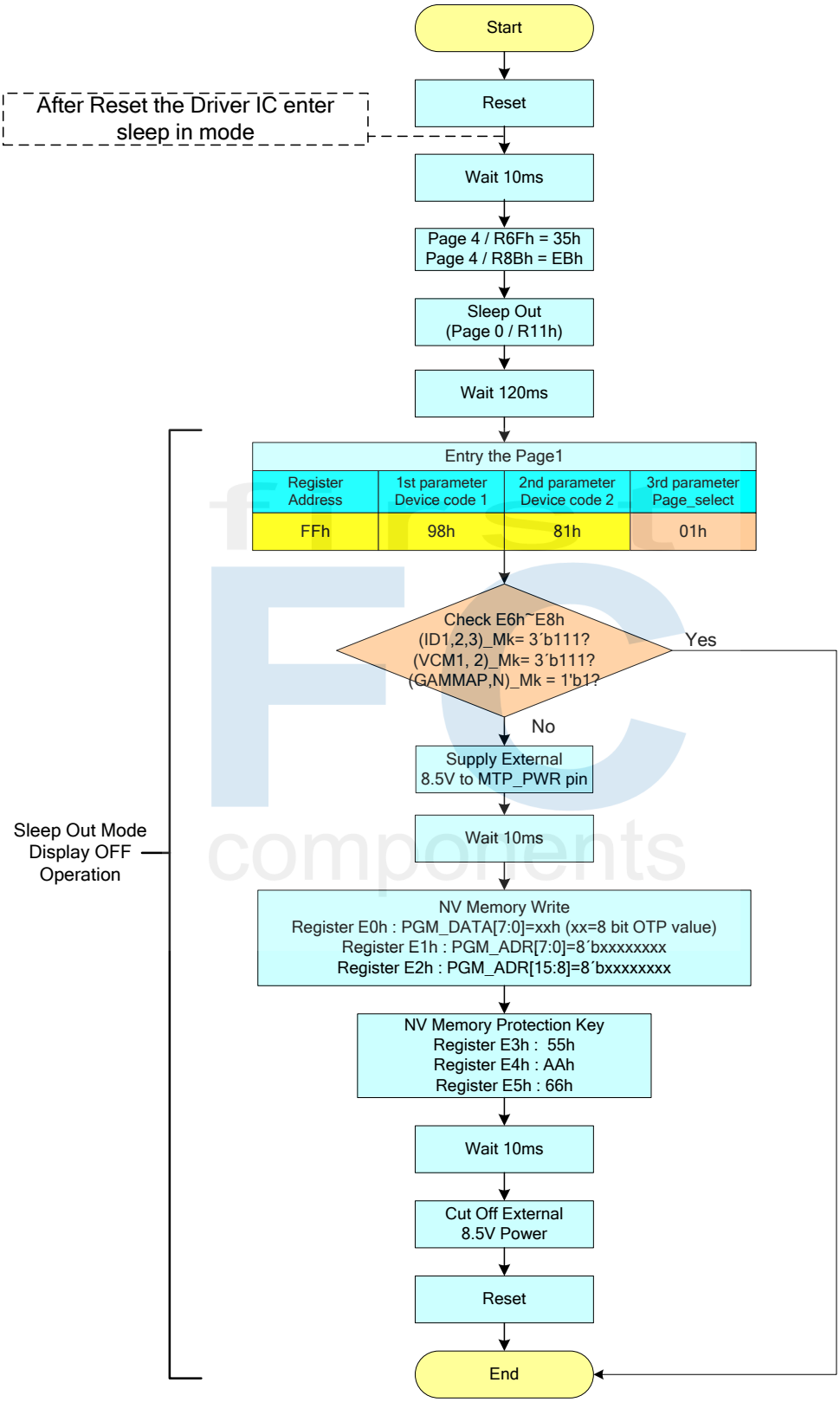
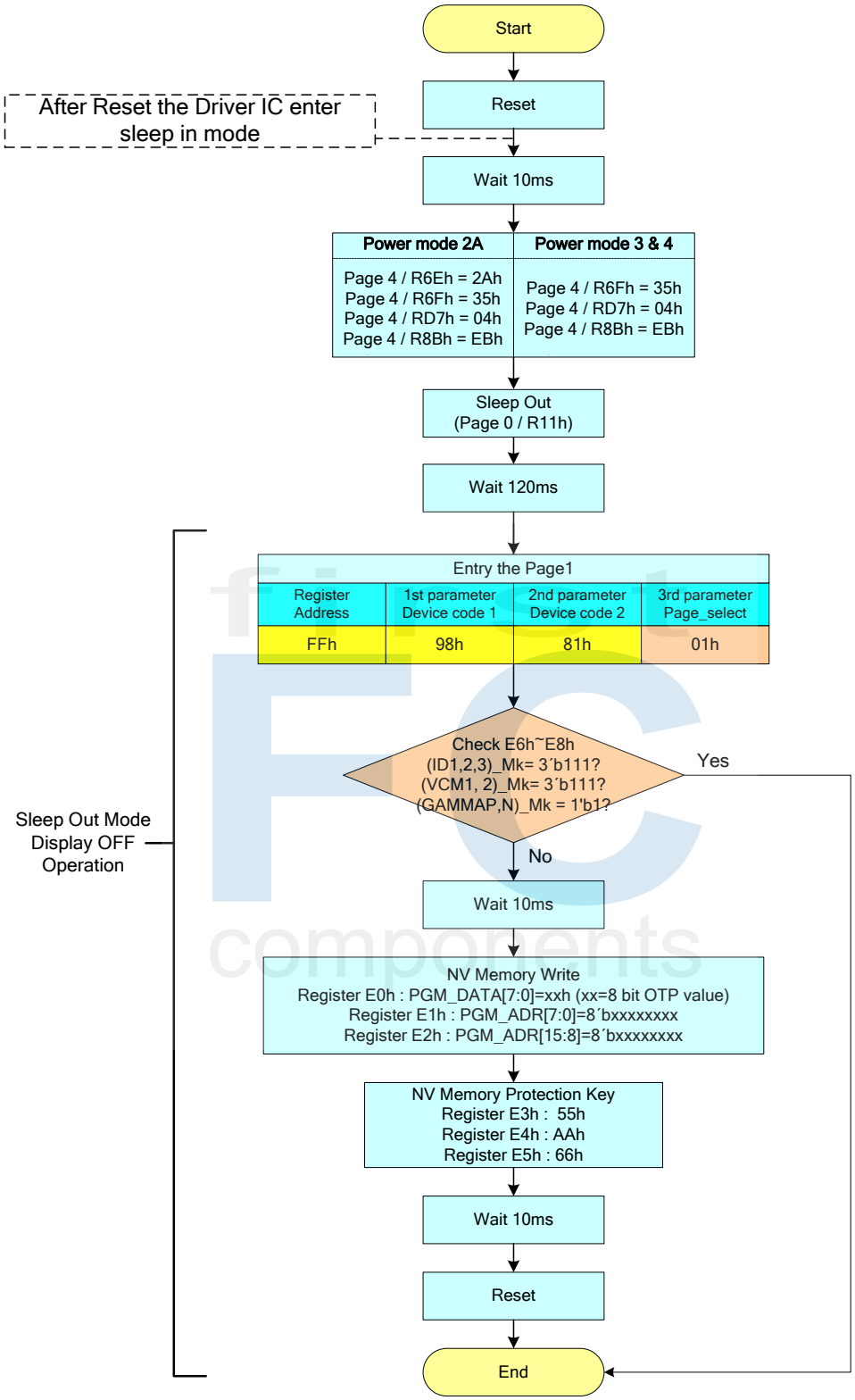


Figure 108: External MTP_PWR Programming Flow

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15.2. Internal VGH Programming Flow



Note: Internal VGH Programming must operate in the Low Power mode.

Figure 109: Internal VGH Programming Flow

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16. Gamma Correction

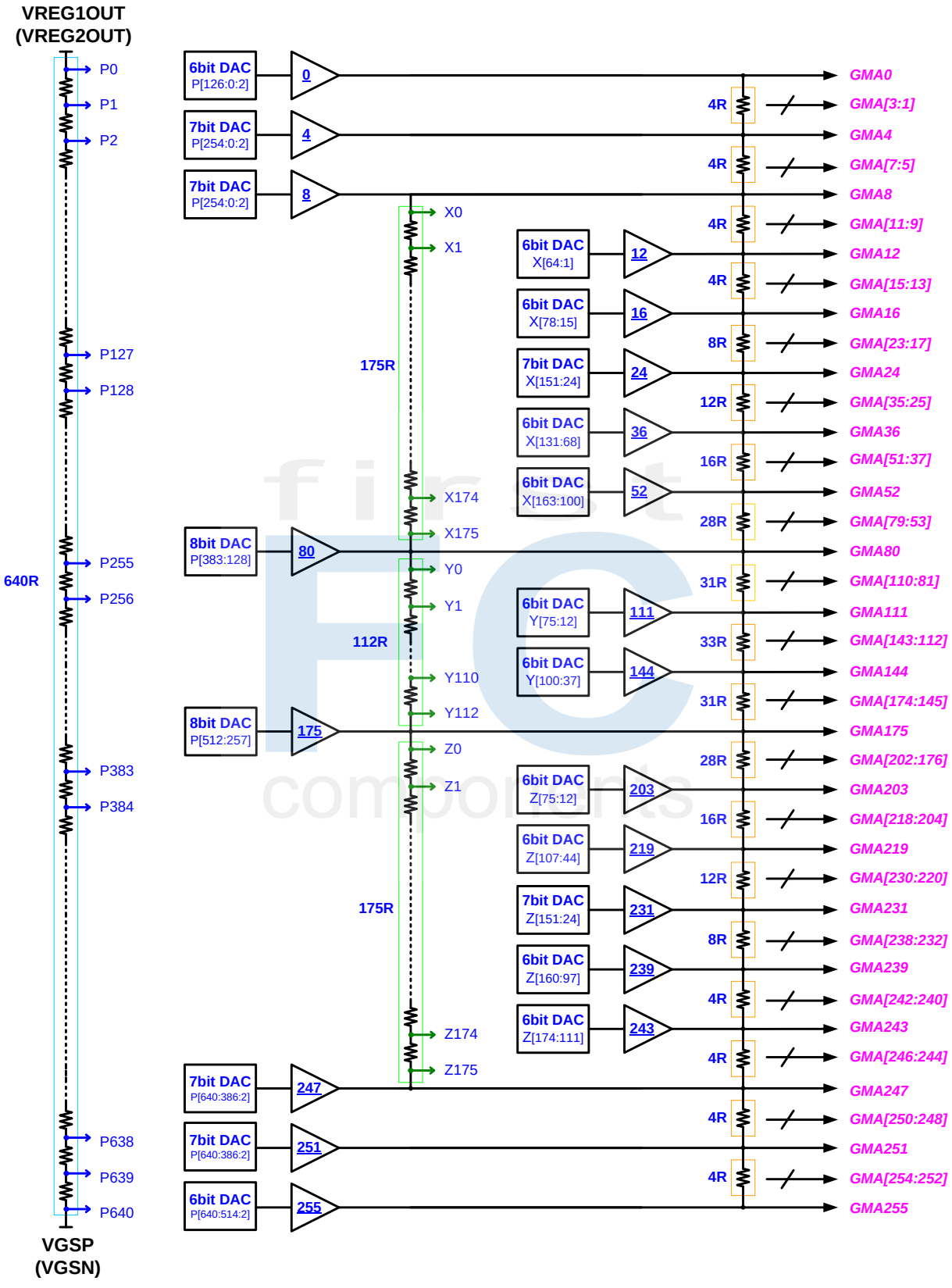


Figure 110: Gamma Architecture

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17. Touch Synchronization Signal

The VS and HS pad of ILI9881C-0D can output the synchronization signals to touch sensing signal for touch panel controller. To use these signals, touch panel controller can receive touch sensing signal while avoiding display changing noise.

These signals are consist of vertical synchronization signal: VSOUT and horizontal synchronization signal: HSOUT. The level of output voltage is VDDI to GND. Each signal can adjust output timing for internal synchronization signal. The high level width of VSOUT is 1 line, and it is adjustable. VSOUT is outputted always, but HSOUT is outputted during displaying only.

(1) VSOUT output Timing

VSOUT output means internal VSYNC is starting point. VSOUT output timing can be adjusted by VSOD register. Unit is 1H.

(2) HSOUT output Timing

HSOUT output means internal source output timing is starting point. HSOUT output timing can be adjusted by HSOD register. And HSOUT high level width can be adjusted by HSOHW register.

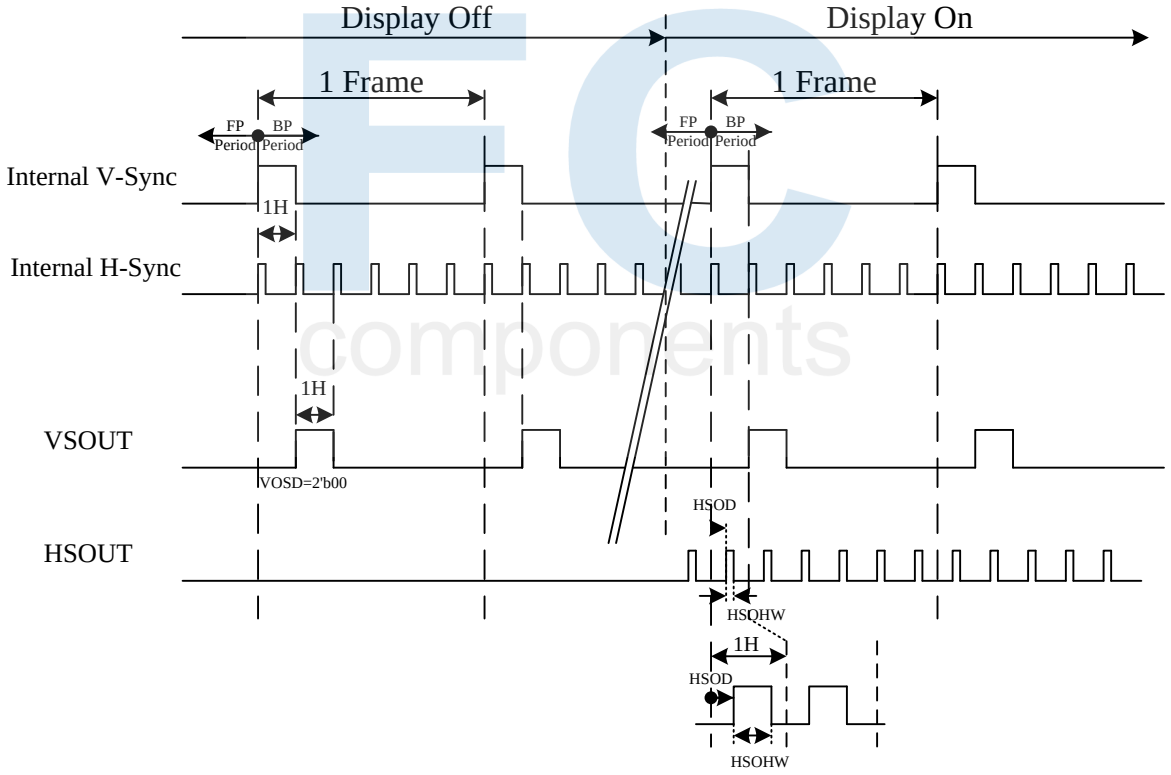


Figure 111: Touch Synchronization Signal

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18. Electrical Characteristics

18.1. Absolute Maximum Ratings

The absolute maximum rating is listed in Table 36. When the ILI9881C-0D is used out of the absolute maximum ratings, it may be permanently damaged. To use the ILI9881C-0D within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9881C-0D will malfunction and cause poor reliability.

Table 36: Absolute Maximum Ratings

Item	Symbol	Unit	Value
Analog Operating Voltage	VCI ~ GND	V	-0.3 ~ +7.0
Analog Operating Voltage	VCIREF ~ GND	V	-0.3 ~ +7.0
Digital Operating Voltage	VDDI ~ GND	V	-0.3 ~ +3.8
Digital Operating Voltage	VCC1 ~ GND	V	-0.3 ~ +7.0
Digital Operating Voltage	VCC2 ~ GND	V	-0.3 ~ +7.0
DSI Operating Voltage	VDDAM ~ GND	V	-0.3 ~ +3.8
OTP Supply Voltage	MTP_PWR ~ GND	V	-0.3 ~ +9.0
Supply Voltage	VSP ~ GND	V	-0.3 ~ +7.0
Supply Voltage	VSN ~ GND	V	0.3 ~ -7.0
Gate Driver High Voltage	VGH ~ GND	V	-0.3 ~ +18
Gate Driver Low Voltage	VGL ~ GND	V	0.3 ~ -18
Driver Supply Voltage	VDDI - VCL	V	≦ 6.6V
Driver Supply Voltage	VGH - VGL	V	≦ 32.0V
Input Voltage	VIN	V	-0.3 ~ VDDI + 0.3
HS Input Voltage	VHSIN	V	-0.3 ~ + 1.65
Operating Temperature	Topr	℃	-30 ~ +70
Storage Temperature	Tstg	℃	-55 ~ +110

Note: *Even if the absolute maximum rating of one of the above parameters is exceeded only for a short while, the quality of the product may be degraded. Therefore, be sure to use the product within the range of the absolute maximum ratings.*

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18.2. DC Characteristics for Panel Driving

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power & Operation Voltage							
Analog operating voltage	VCI	-	2.5	2.8	6.6	V	
Analog operating voltage	VCIREF		2.5	2.8	6.6	V	
Digital operating voltage	VDDI	-	1.65	2.8	3.6	V	
Digital operating voltage	VCC1		1.65	2.8	6.6	V	
Digital operating voltage	VCC2		1.65	2.8	6.6	V	
DSI operating voltage	VDDAM	-	1.65	1.8	3.6	V	
OTP Supply voltage	MTP_PWR	-	8.4	8.5	8.6	V	
Analog operating voltage	VSP	-	4.5		6.6	V	
Analog operating voltage	VSN	-	-6.6		-4.5	V	
Logic High level input voltage	VIH	-	0.7*VDDI		VDDI	V	Note1
Logic Low level input voltage	VIL	-	-0.3		0.3*VDDI	V	Note1
Logic High level output voltage TE , LEDPWM	VOH	IOH = -1.0mA	0.8*VDDI		VDDI	V	Note1
Logic Low level output voltage TE , LEDPWM	VOL	IOL = +1.0mA	0		0.2*VDDI	V	Note1
Gate Driver High Voltage	VGH	-	8.0	-	18	V	
Gate Driver Low Voltage	VGL	-	-18.0	-	-7.0	V	
Driver Supply Voltage	-	|VGH-VGL|	15	-	32	V	
VCOM Operation							
DC VCOM Amplitude Voltage	VCOM	-	-4.0	-	0	V	Note3
Source Driver							
Source Output Range	VSOUT(+)	-	0.3	-	VREG1OUT-0.1	V	Note4
	VSOUT(-)	-	VREG2OUT +0.1	-	-0.3	V	Note4
Positive Gamma Reference Voltage	VREG1OUT	-	3.5	-	VSP-0.5 (VSP<=6.1) 5.6 (VSP>6.1)	V	
Negative Gamma Reference Voltage	VREG2OUT	-	VSN+0.5 (VSN>=-6.1) -5.6 (VSN<-6.1)	-	-3.5	V	
Source Output Setting Time	Tr	Below with 99% precision	-	10	-	uS	Note3.4
Output Deviation Voltage (Source Output channel)	Vdev	Sout>=4.2V Sout<=0.8V	-	-	20	mV	Note3
		4.2V>Sout>0.8V	-	-	15	mV	
Output Offset Voltage	VOFFSET	-	-	-	35	mV	Note3
Standby mode current consumption							
Sleep In mode	I(VDDI SLP IN)	Ta = 25 °C VCI=2.8V VDDI=1.8V	-	35	-	uA	
	I(VCI SLP IN)		-	25	-	uA	

Notes:

1. Ta = -30 to 70 °C (to 85 °C no damage) , VCI = 2.5V to 6.6V, VDDI = 1.65V to 3.6V

2. Supply digital VDDI voltage equal or less than analog VCI voltage.

3. Source channel loading = 9KΩ,70pF/channel

4. The maximum value is between with Note 3 and Gamma setting value

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18.3. DSI DC Characteristics

The DSI uses different state codes which depend on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined in the following table.

State Code	Line DC Voltage Levels	
	CLOCK_P or DATA_P	CLOCK_N or DATA_N
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	High (LP)
LP-10	High (LP)	Low (LP)
LP-11	High (LP)	High (LP)

Note: *Ta = -30℃ to 70℃ (to +85℃ no damage)*

18.3.1. DC Characteristics for DSI LP Mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined in the table below: DC Characteristics for the DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned in the condition column. Other logical levels in the table are for MCU interface.

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Logic 1 input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic 0 input voltage	V_{ILLPCD}	LP-CD	0.0	-	200	mV
Logic 1 input voltage	V_{IHLPRX}	LP-RX (CLK, D0 ,D1, D2, D3)	880	-	1350	mV
Logic 0 input voltage	V_{ILLPRX}	LP-RX (CLK, D0 ,D1, D2, D3)	0.0	-	550	mV
Logic 0 input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0.0	-	300	mV
Logic 1 output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic 0 output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic 1 input current	I_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic 0 input current	I_{IL}	LP-CD, LP-RX	-10	-	-	uA

Notes:

1.Ta = -30℃ to 70℃ (to +85℃ no damage)

2. DSI High Speed mode is off.

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18.3.2. Spike/Glitch Rejection

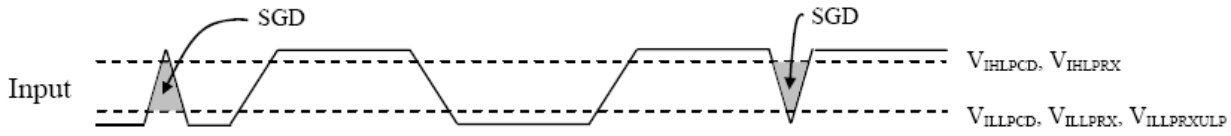


Figure 112: Spike/Glitch Rejection

Notes:

1. *A spike/glitch can be rejected when the Peak Interference Amplitude is 200mV (at maximum) and Interference Frequency is 450MHz (at the very least).*
2. *n = 0, 1, 2 and 3.*

Table 37: Spike/Glitch Rejection

Spike/Glitch Rejection – DSI					
Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N, DnP/N	SGD	Input pulse rejection for DSI	-	300	Vps

first FC components

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18.3.3. DC Characteristics for DSI HS mode

Parameter	Symbol	Condition	Specification			Unit
Input Common Mode Voltage for Clock	V_{CMCLK}	CLKP/N Note 2, Note 3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DnP/N Note 2, Note 3, Note 5	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	CLKP/N Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DnP/N Note 4, Note 5	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	CLKP/N	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DnP/N Note 5	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	CLKP/N	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DnP/N Note 5	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	CLKP/N	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DnP/N Note 5	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	CLKP/N, DnP/N Note 3, Note 5	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	CLKP/N, DnP/N Note 3, Note 5	-	-	460	mV
Differential Termination Resistor	R_{TERM}	CLKP/N, DnP/N Note 5	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	CLKP/N, DnP/N Note 5	-	-	450	mV
Termination Capacitor	C_{TERM}	CLKP/N, DnP/N Note 5, Note 6	-	-	60	pF

Notes:

1. Ta = -30℃ to 70℃ (to +85℃ no damage) , VCI = 2.5V to 6.6V, VDDI = 1.65V to 3.6V

2. Includes 50mV (-50mV to 50mV) ground difference

3. Without VCMRCLKM450/VCMRDATAM450

4. Without 50mV (-50mV to 50mV) ground difference

5. n = 0, 1, 2 and 3

6. For higher bit rates, a 14pF capacitor will be needed to meet the common-mode return loss specification.

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The DSI receiver (HS mode) understands that there is logical 1 (= HS-1) when a differential voltage is more than VTHH (CLKP/DnP). The DSI receiver (HS mode) understands that there is logical 0 (= HS-0) when a differential voltage is more than VTHL (CLKN/DnN). There is undefined state if the differential voltage is less than VTHH (CLKP/DnP) and less than VTHL (CLKN/DnN). A reference figure is below.

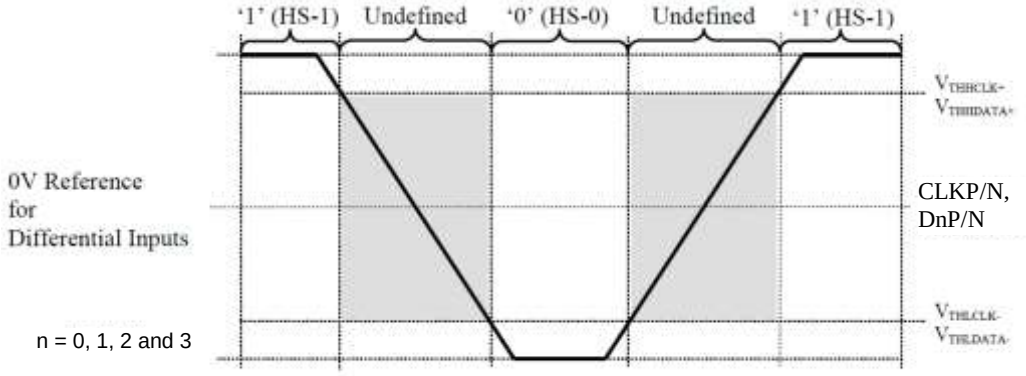
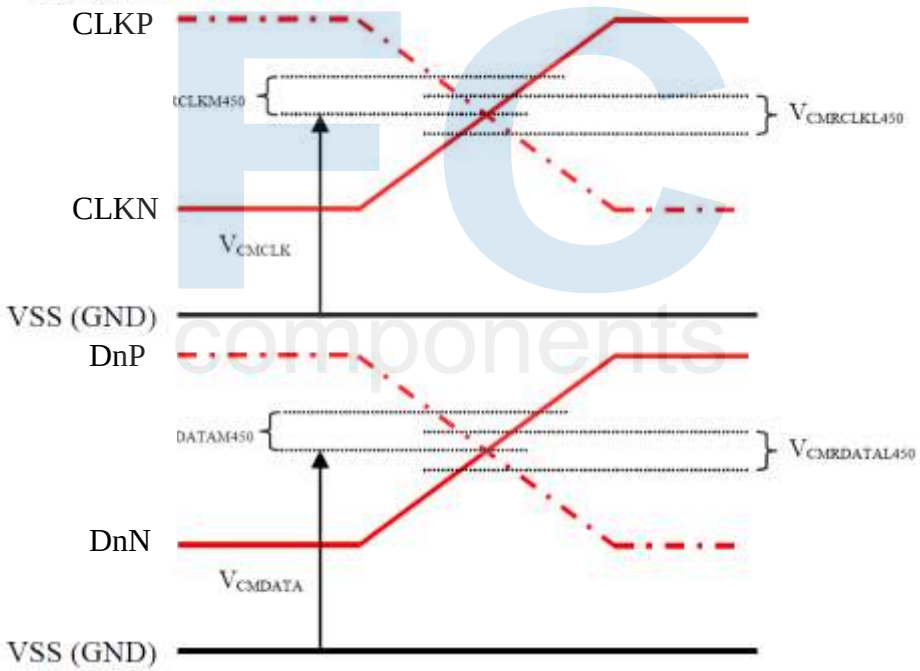


Figure 113: Differential Inputs Logical 0 and 1, Threshold High/Low, Differential Voltage Range



Note: *n = 0, 1, 2 and 3*

Figure 114: Common Mode Voltage on Clock and Data Channels

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The termination resistor (RTERM) of the differential DSI receiver can be driven to two different states by the receiver:

- Low Power (LP) mode when the termination resistor is not connected between differential inputs (CLKP <=> CLKN or D0P <=> D0N or D1P <=> D2N or D2P <=> D3N or D1P <=> D3N)
- High Speed (HS) mode when the termination resistor is connected between differential inputs (CLKP <=> CLKN or D0P <=> D0N or D1P <=> D2N or D2P <=> D3N or D1P <=> D3N)

The termination switch (HS/LP), when the termination resistor is not connected, is illustrated below.

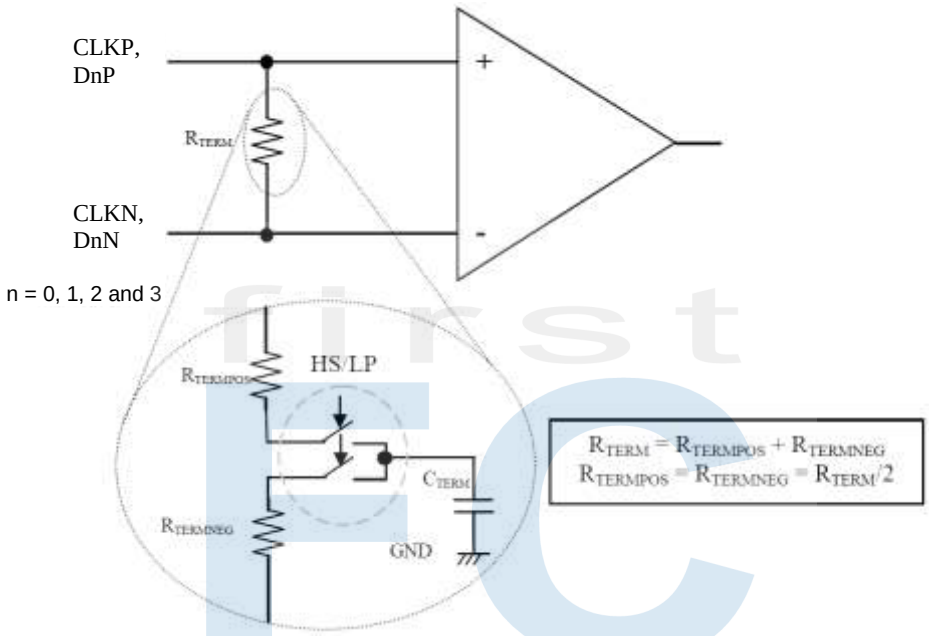


Figure 115: Differential Pair Termination Resistor on the Receiver Side

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18.4. AC Characteristics

18.4.1. DSI Timing Characteristics

18.4.2. High Speed Mode – Clock Channel Timing

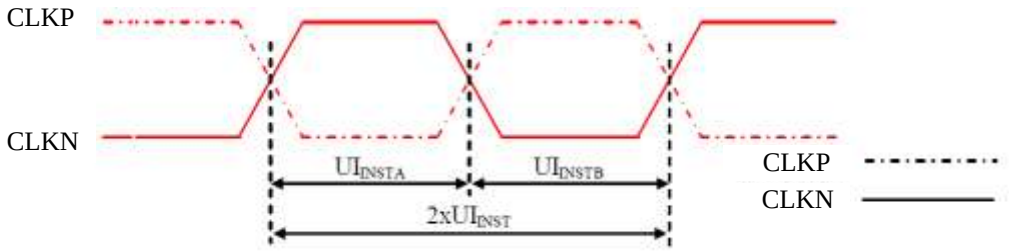


Figure 116: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	*Note 2*	25	ns
CLKP/N	UI_{INSTA},UI_{INSTB} (Note 1)	UI instantaneous Half	*Note 2*	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps

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18.4.3. High Speed Mode – Data Clock Channel Timing

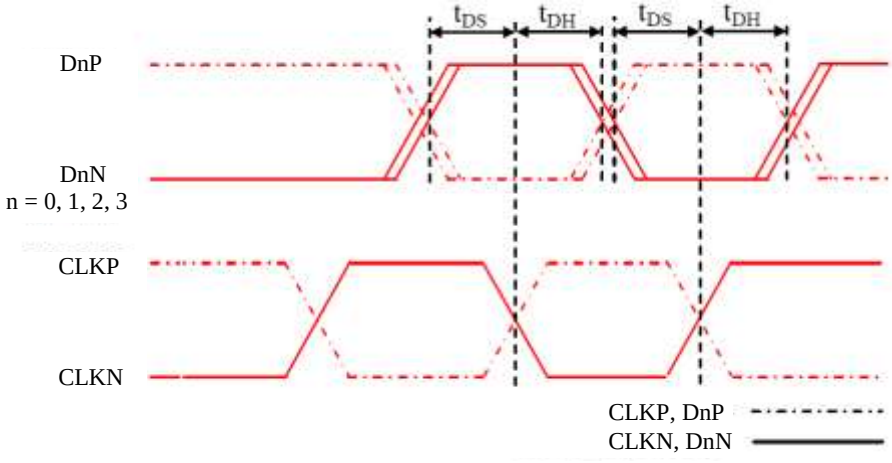


Figure 117: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0,1,2,3	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

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18.4.4. High Speed Mode – Rising and Falling Timings

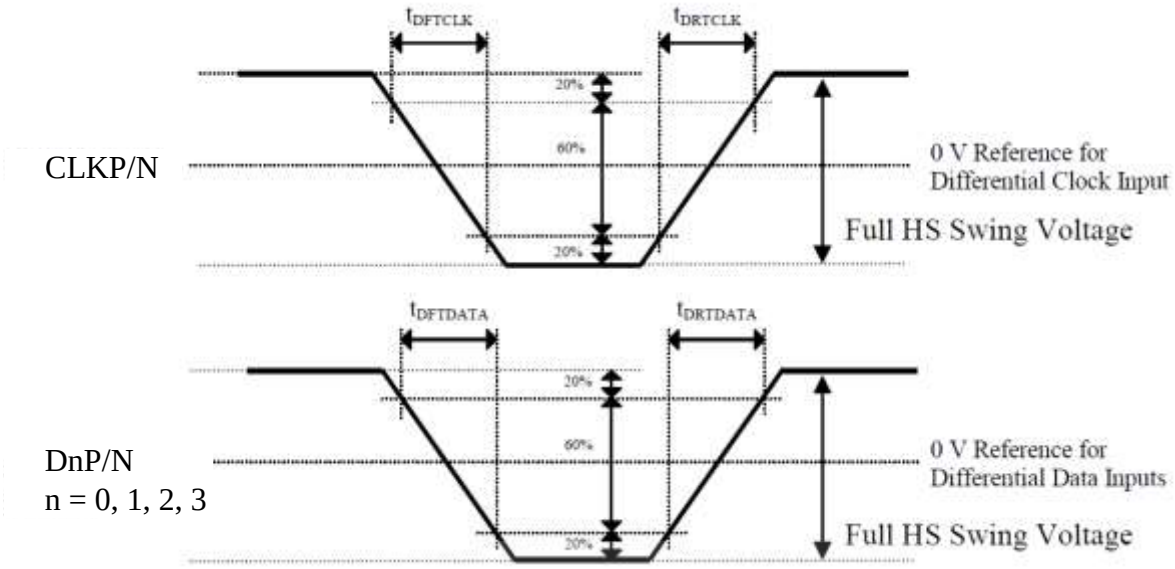


Figure 118: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0,1,2,3	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0,1,2,3	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

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18.4.5. Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C-0D) are illustrated for reference purposes below.

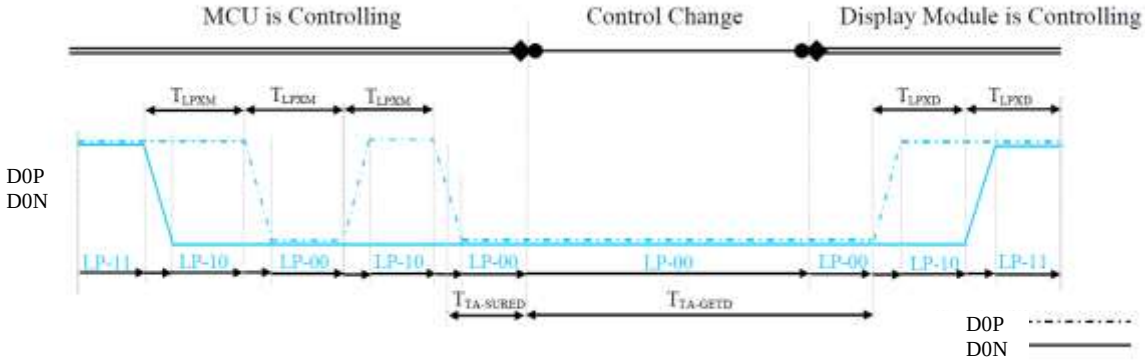


Figure 119: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C-0D) to the MCU are illustrated for reference purposes below.

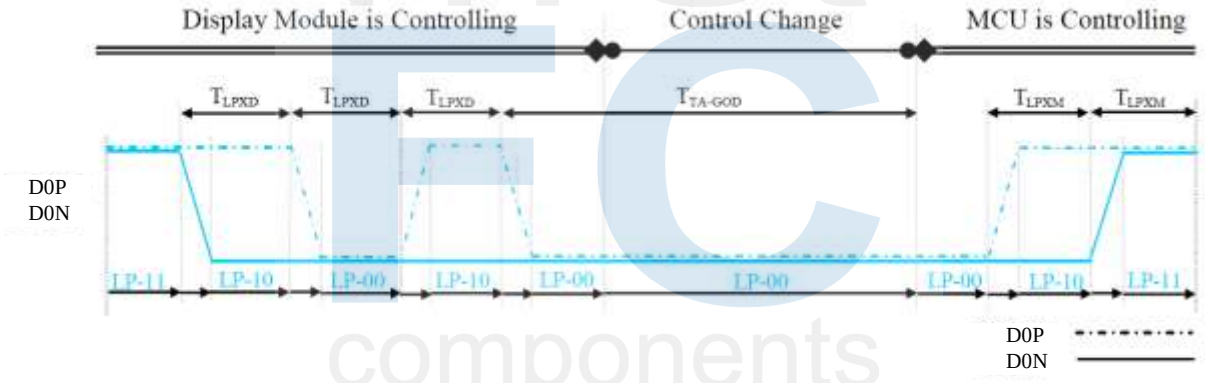


Figure 120: BTA from the Display Module to the MCU

Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU ➔ Display Module (ILI9881C-0D)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C-0D) ➔ MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C-0D) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C-0D)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

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18.4.6. Data Lanes from Low Power Mode to High Speed Mode

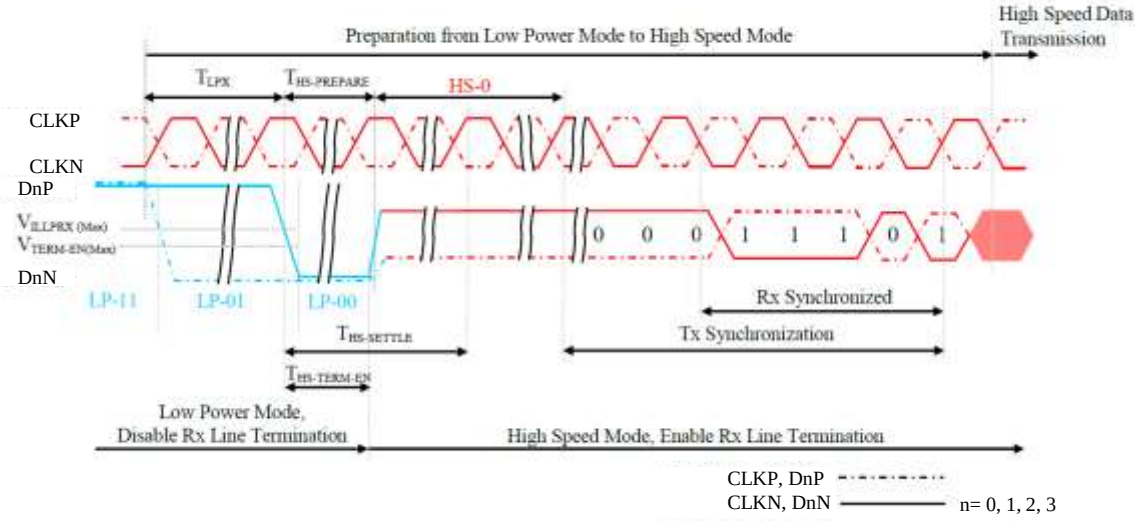


Figure 121: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0,1,2,3	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0,1,2,3	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0,1,2,3	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

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18.4.7. Data Lanes from High Speed Mode to Low Power Mode

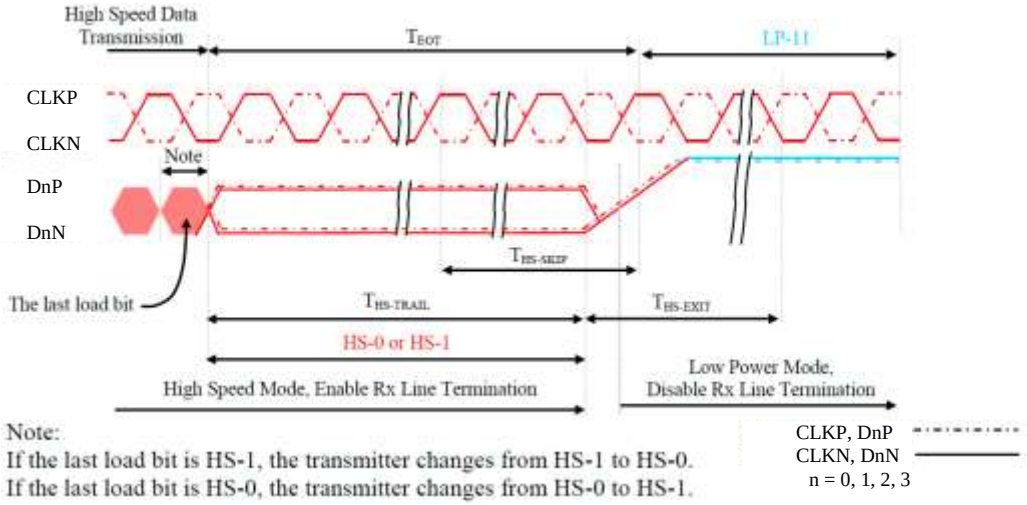


Figure 122: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0,1,2,3	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C-0D) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0,1,2,3	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns
DnP/N, n = 0,1,2,3	$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	Max(8*UI,60ns+4*UI)	-	ns

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18.4.8. DSI Clock Burst – High Speed Mode to/from Low Power Mode

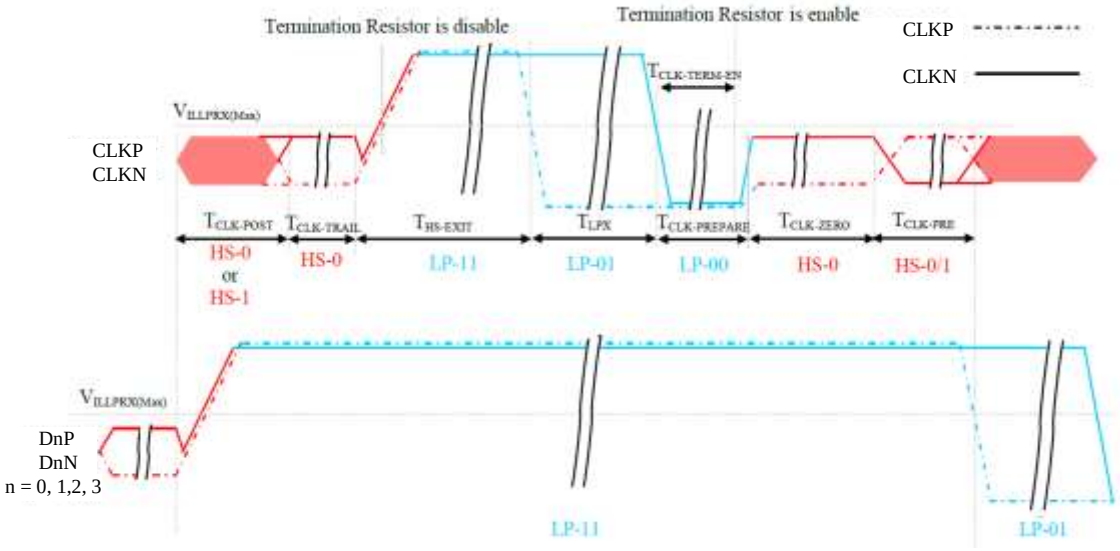


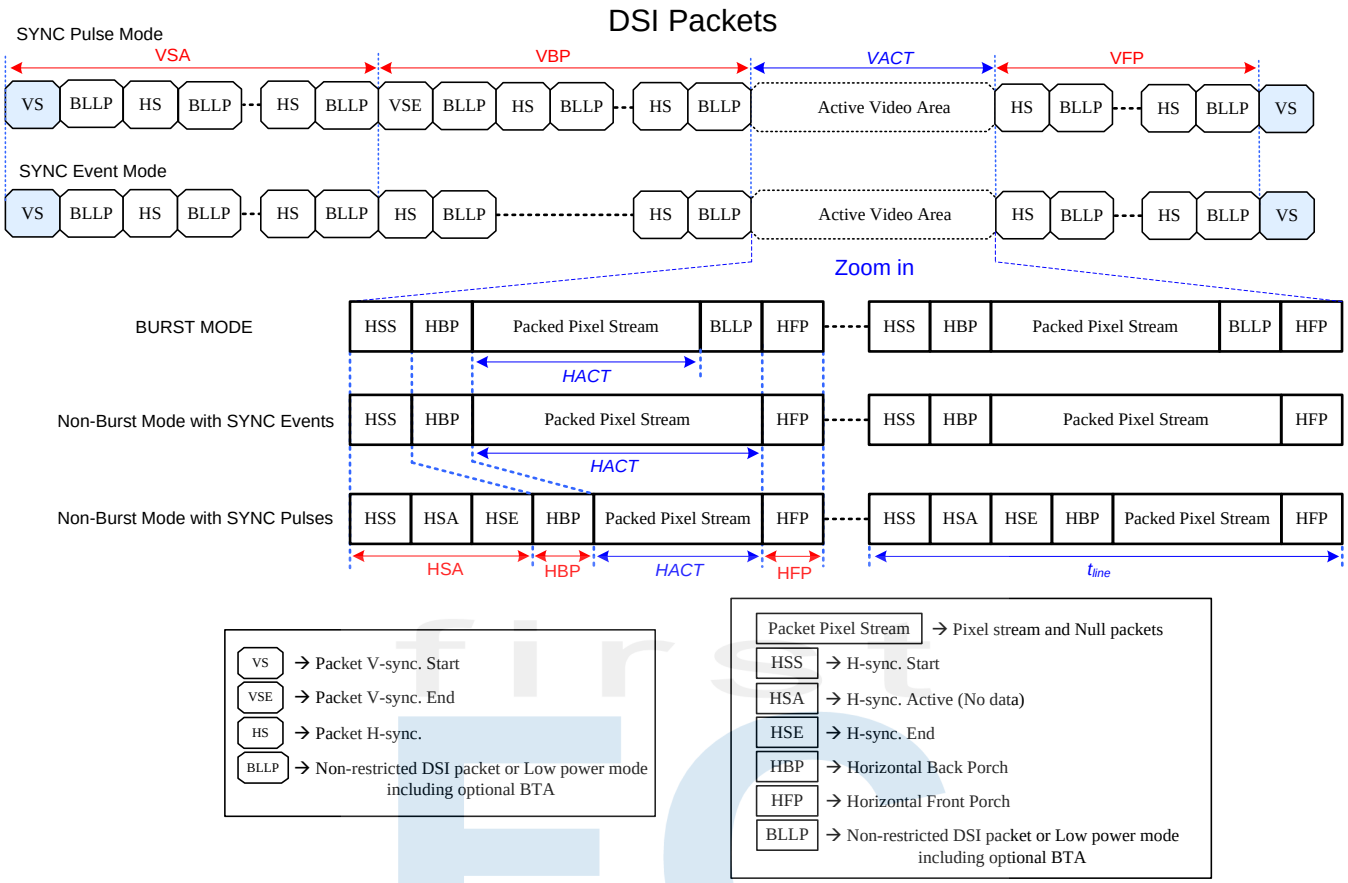
Figure 123: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

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18.4.9. Timing for DSI video mode



VS → Packet V-sync. Start
VSE → Packet V-sync. End
HS → Packet H-sync.
BLLP → Non-restricted DSI packet or Low power mode including optional BTA

Packet Pixel Stream → Pixel stream and Null packets
HSS → H-sync. Start
HSA → H-sync. Active (No data)
HSE → H-sync. End
HBP → Horizontal Back Porch
HFP → Horizontal Front Porch
BLLP → Non-restricted DSI packet or Low power mode including optional BTA

Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	2 (Note 6)	-	-	Line
Vertical Back Porch	VBP	14 (Note 6)	-	-	Line
Vertical Front Porch	VFP	8 (Note 6)	-	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	2	-	-	Pixel
Horizontal Porch period	HSA + HBP + HFP	1.6	-	-	us
Active pixels per line	HACT	-	720	-	Pixel
Bit rate	BR_{bps}	385		Note 5	Mbps/lane

1 UI=1/Bit rate

HSA(pixel)= (tHSA*lane number) / (UI* pixel format)

HBP(pixel)= (tHBP*lane number) / (UI* pixel format)

HFP(pixel)= (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Example：BR_{bps} = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, $Lane_{num}$=4(lane), Pixel Format=24(bit).

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Note:

1. $Lane_{num}$: Date lane of MIPI-DSI.
2. Pixel Format: Please reference to “4.1DSI System Interface”.
3. The formula exists slightly error because of the host-transmission way.
4. The best frame rate setting： 2 data lanes：50~60 Hz / 3 data lanes：50~70 Hz / 4 data lanes：50~70 Hz.
5. Please reference to “Table 39: Limited Clock Channel Speed”.
6. The minimum values of this table mean the limitation of IC without considering the panel GIP. The actual values of VSA, VBP and VFP will be changed by different panel GIP setting.

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18.4.10. Reset Timing

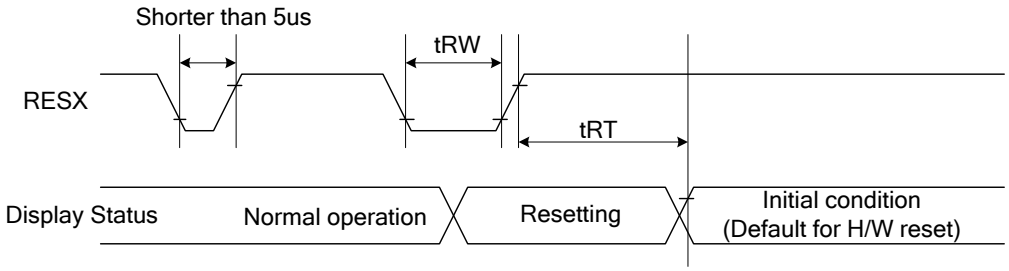


Figure 124: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

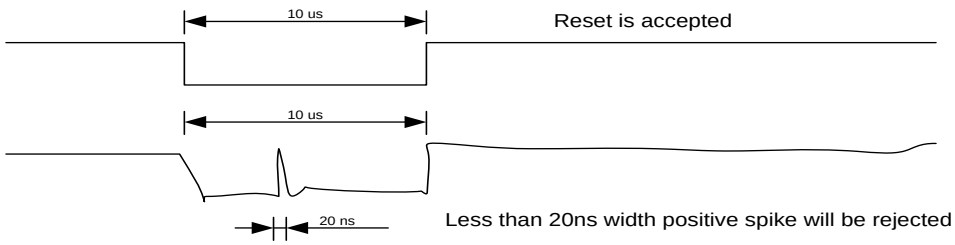


Figure 125: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

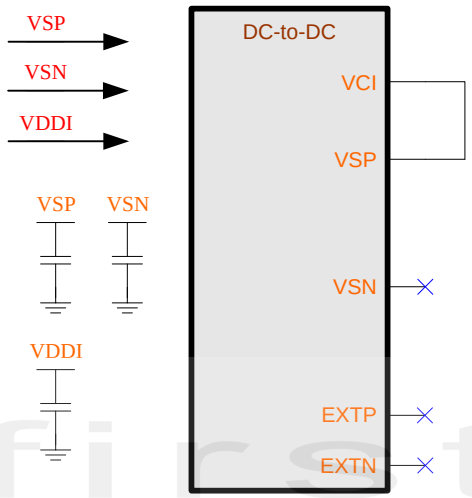
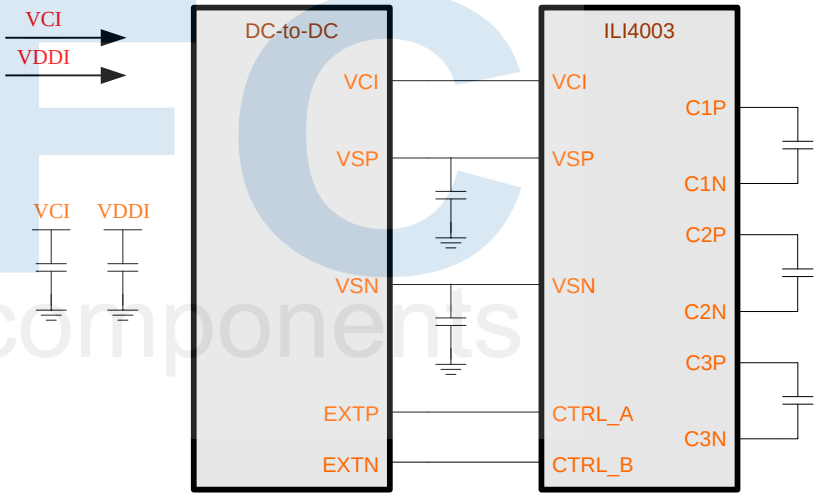
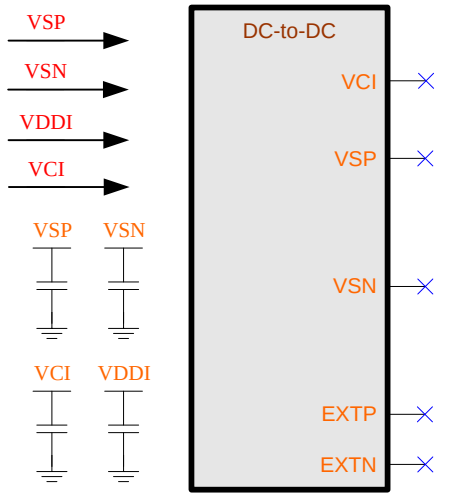
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19. Panel Application

19.1. Input Power Type

ILI9881C-0D supports 3 kinds of input power type as shown below.

Table 49: Different Input Power Type

Setting	Input Power Type
Power Mode 2A BOOSTM[2:0] = 1h DI_PWR_REG = 0h	
Power Mode 3 BOOSTM[2:0] = 2h DI_PWR_REG = don't care	
Power Mode 4 BOOSTM[2:0] = 1h DI_PWR_REG = 1h	

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19.2. Power Mode 2A (BOOSTM[2:0] = 1h, DI_PWR_REG = 0h)

19.2.1. Power Structure

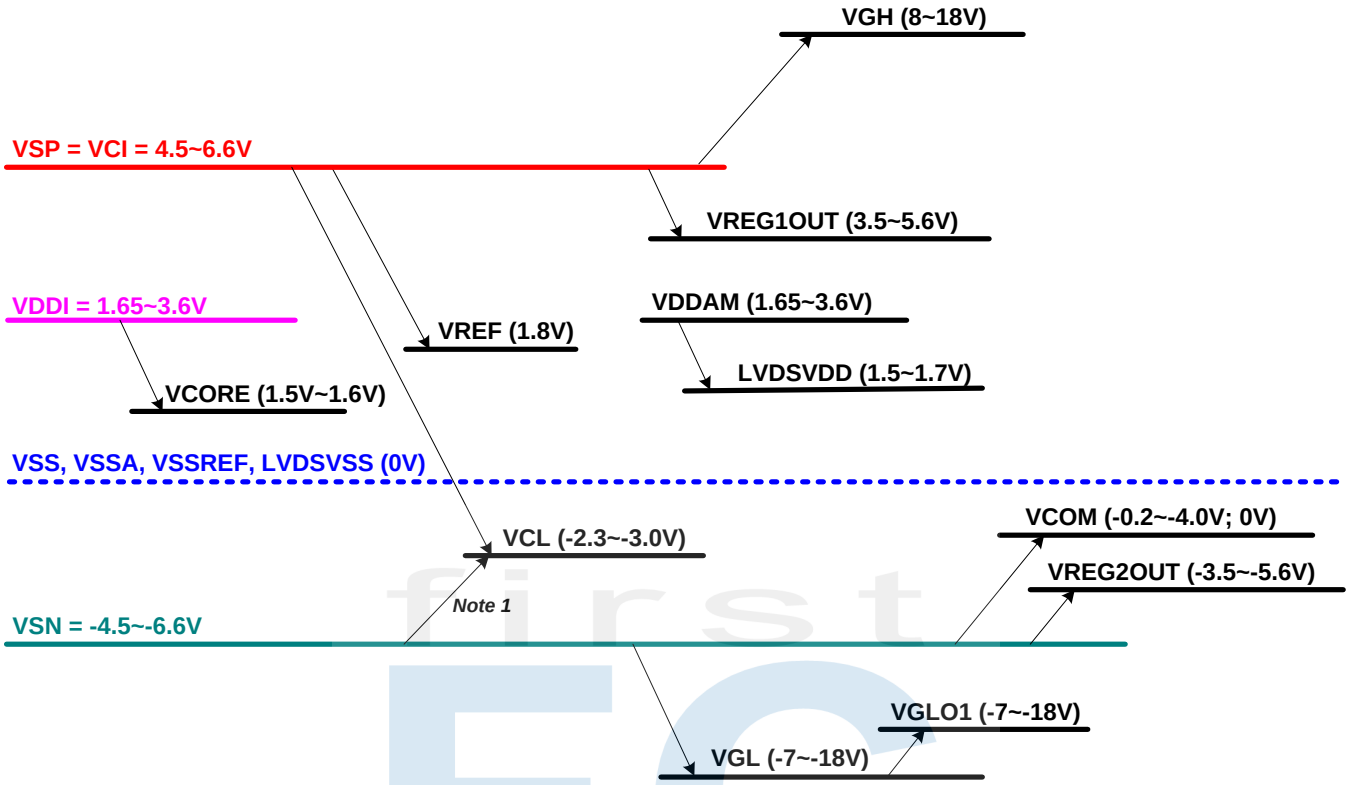


Figure 126: Power Structure of Power Mode 2A

Notes:

1. *Please refer to"5.7.12 Power Control 3 (6Fh)".*
2. *The VREG1OUT, VREG2OUT, VCOM, VGH, VGL and VCL output voltage levels are lower than their theoretical levels (Ideal voltage levels) due to the current consumption at respective outputs.*

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19.2.2. Reference Circuit

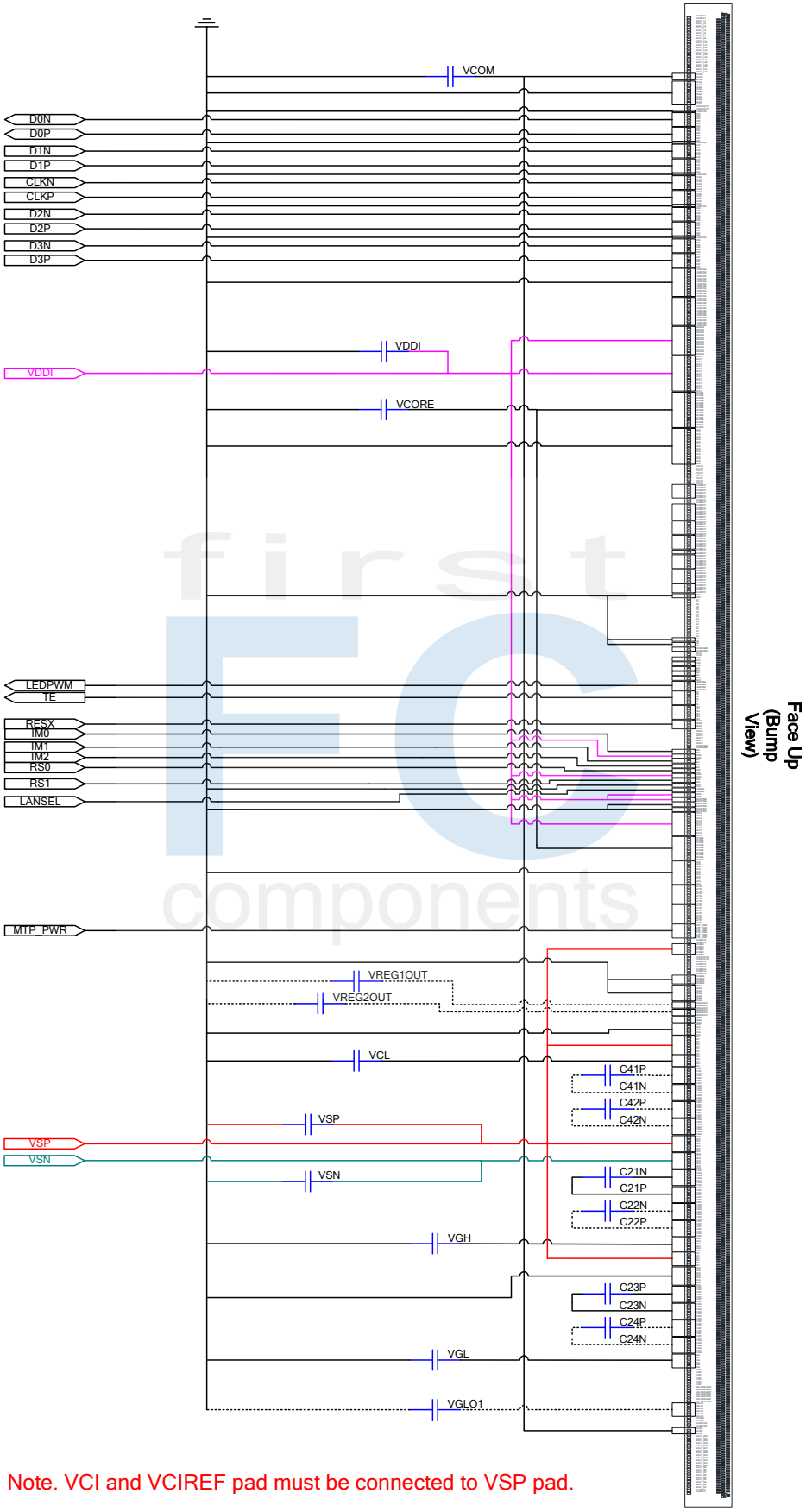


Figure 127: Reference Circuit of Power Mode 2A

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19.2.3. External Component

Table 50: External Component table of Power Mode 2A

N0.	Pad Name	Typical Value	Note	Reference Command (page)
1	VDDI	1.0uF / 6.3V	I/O and Digital Power	
2	VSP	2.2~4.7uF / 10V	Analog Power	
3	VSN	4.7uF / 10V	Analog Power	
4	VCORE	2.2uF / 6.3V		
5	VCL	1.0uF / 6.3V		
6	VREG1OUT	1.0uF / 10V	Optional	Register Page 4_R7Ah (page.231)
7	VREG2OUT	1.0uF / 10V	Optional	Register Page 4_R7Ah (page.231)
8	VCOM	2.2uF / 6.3V		
9	VGH	1.0uF / 25V		
10	VGL	1.0uF / 25V		
11	VGLO1	1.0uF / 25V	Optional (if not used)	Register Page 4_R6Fh (page.229)
12	C21P/C21N	1.0uF / 16V		
13	C22P/C22N	1.0uF / 25V	Optional	Register Page 4_R6Fh (page.229)
14	C23P/C23N	1.0uF / 16V		
15	C24P/C24N	1.0uF / 25V	Optional	Register Page 4_R6Fh (page.229)
16	C41P/C41N	1.0uF / 6.3V	Optional	Register Page 4_R6Fh (page.229)
17	C42P/C42N	1.0uF / 6.3V	Optional	Register Page 4_R6Fh (page.229)

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19.3. Power Mode 3 (BOOSTM[2:0] = 2h, DI_PWR_REG = don't care)

19.3.1. Power Structure

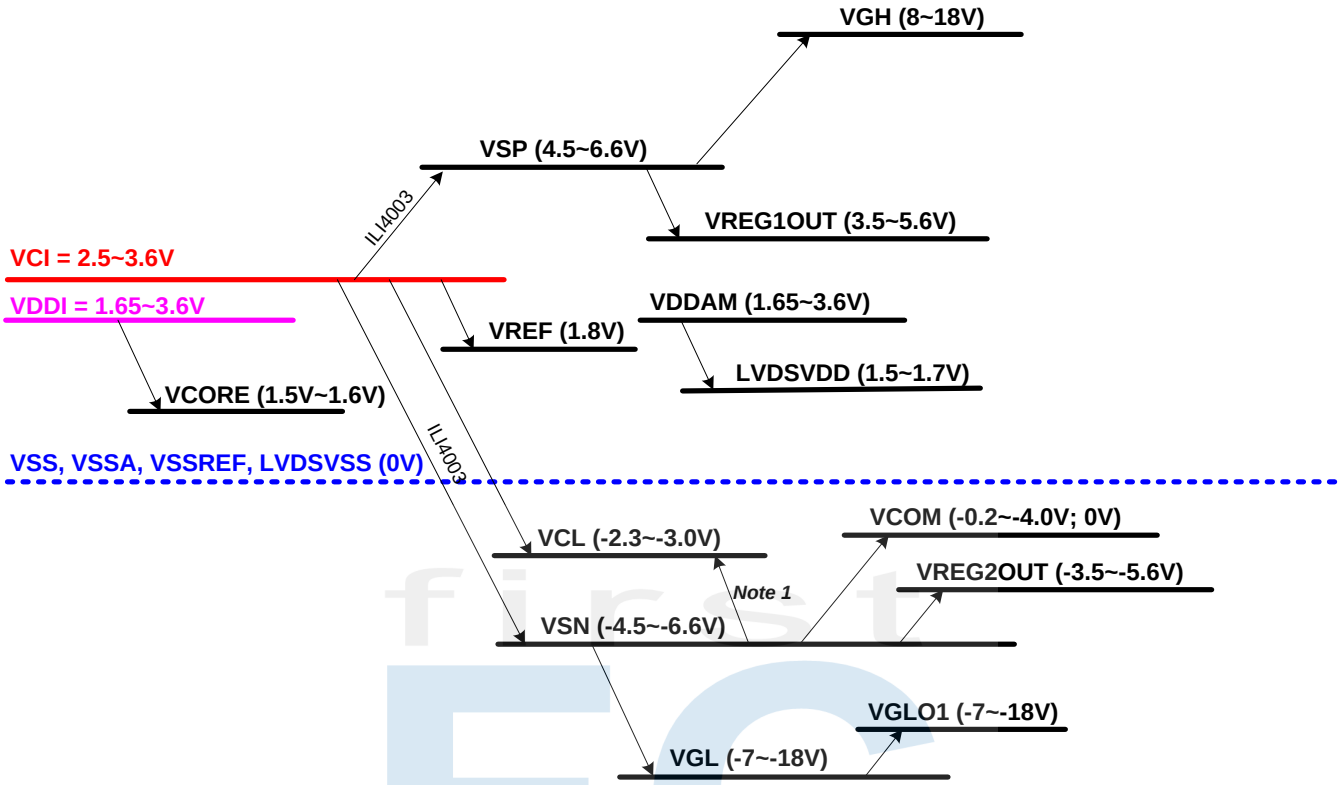


Figure 128: Power Structure of Power Mode 3

Notes:

1. *Please refer to"5.7.12 Power Control 3 (6Fh)".*
2. *The VSP, VSN, VREG1OUT, VREG2OUT, VCOM, VGH, VGL and VCL output voltage levels are lower than their theoretical levels (Ideal voltage levels) due to the current consumption at respective outputs.*

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19.3.2. Reference Circuit

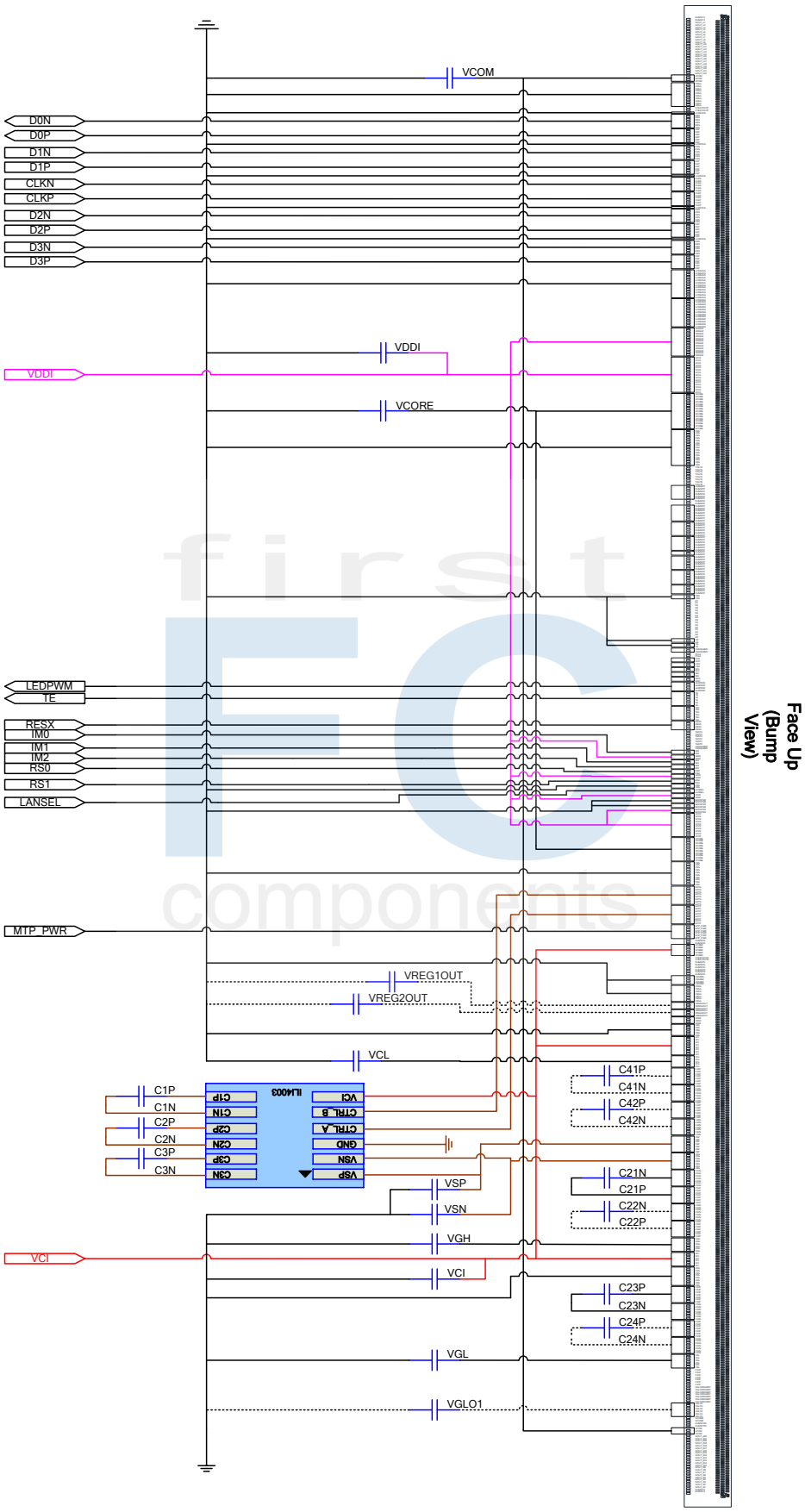


Figure 129: Reference Circuit of Power Mode 3

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19.3.3. External Component

Table 51: External Component table of Power Mode 3

N0.	Pad Name	Typical Value	Note	Reference Command (page)
1	VCI	1.0uF / 6.3V	Analog Power	
2	VDDI	1.0uF / 6.3V	I/O and Digital Power	
3	VSP	2.2~4.7uF / 10V		
4	VSN	2.2~4.7uF / 10V		
5	VCORE	2.2uF / 6.3V		
6	VCL	1.0uF / 6.3V		
7	VREG1OUT	1.0uF / 10V	Optional	Register Page 4_R7Ah (page.231)
8	VREG2OUT	1.0uF / 10V	Optional	Register Page 4_R7Ah (page.231)
9	VCOM	2.2uF / 6.3V		
10	VGH	1.0uF / 25V		
11	VGL	1.0uF / 25V		
12	VGLO1	1.0uF / 25V	Optional (if not used)	Register Page 4_R6Fh (page.229)
13	C21P/C21N	1.0uF / 16V		
14	C22P/C22N	1.0uF / 25V	Optional	Register Page 4_R6Fh (page.229)
15	C23P/C23N	1.0uF / 16V		
16	C24P/C24N	1.0uF / 25V	Optional	Register Page 4_R6Fh (page.229)
17	C41P/C41N	1.0uF / 6.3V	Optional	Register Page 4_R6Fh (page.229)
18	C42P/C42N	1.0uF / 6.3V	Optional	Register Page 4_R6Fh (page.229)
19	Q1		ILI4003	
20	C1P/C1N	2.2uF / 6.3V		
21	C2P/C2N	2.2uF / 6.3V		
22	C3P/C3N	2.2uF / 6.3V		

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19.4. Power Mode 4 (BOOSTM[2:0] = 1h, DI_PWR_REG = 1h)

19.4.1. Power Structure

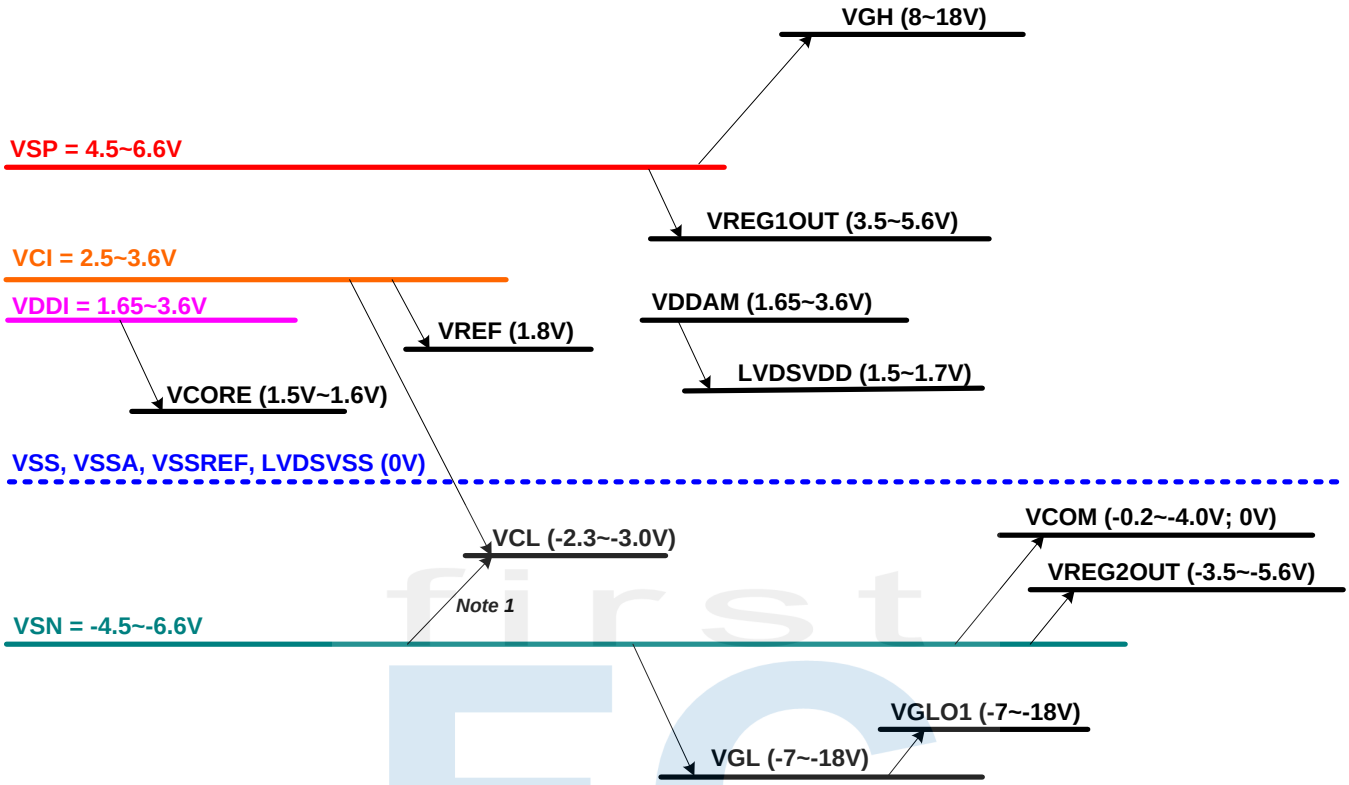


Figure 130: Power Structure of Power Mode 4

Notes:

1. *Please refer to"5.7.12 Power Control 3 (6Fh)".*
2. *The VREG1OUT, VREG2OUT, VCOM, VGH, VGL and VCL output voltage levels are lower than their theoretical levels (Ideal voltage levels) due to the current consumption at respective outputs.*

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19.4.2. Reference Circuit

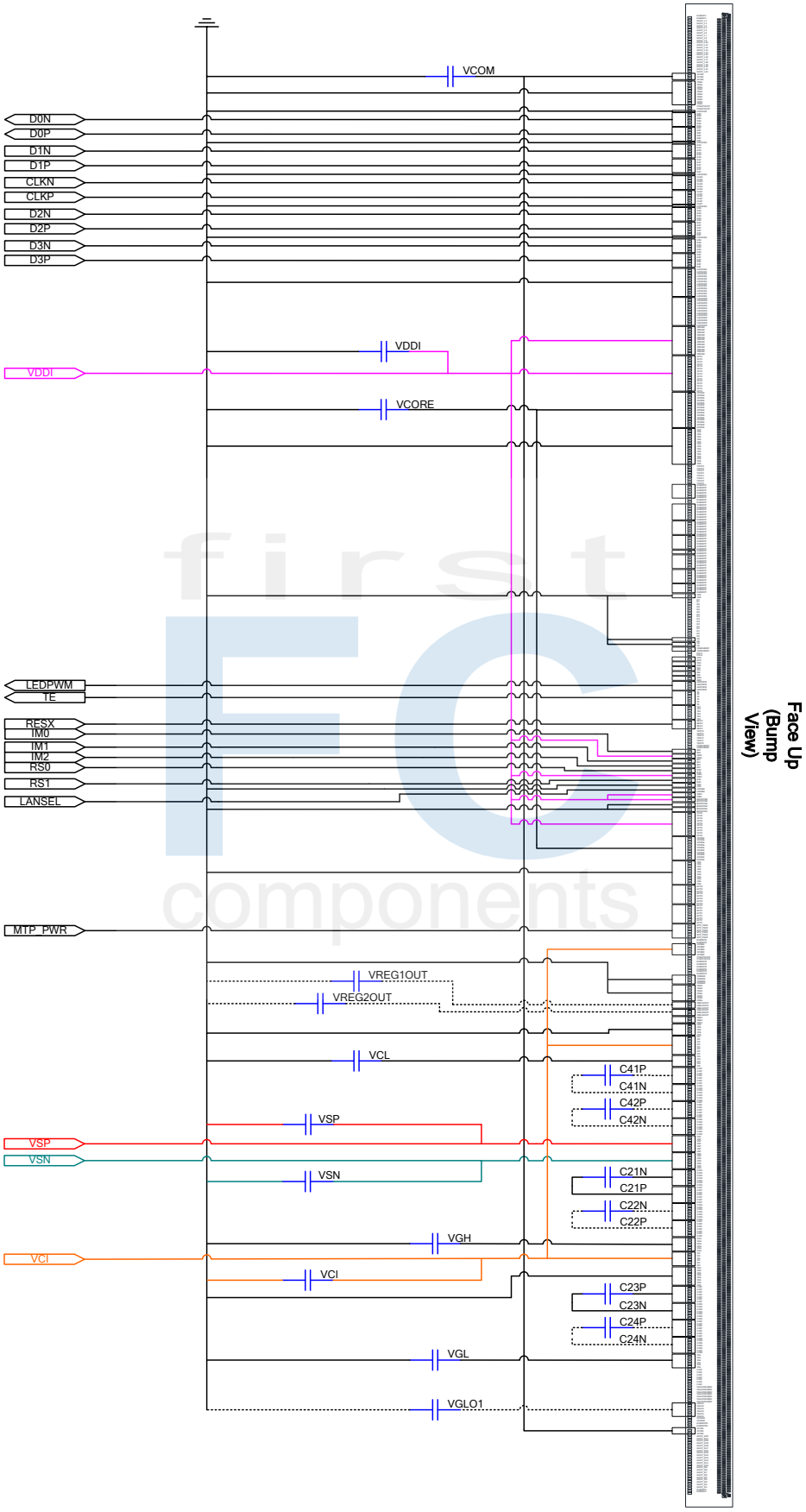


Figure 131: Reference Circuit of Power Mode 4

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19.4.3. External Component

Table 52: External Component table of Power Mode 4

N0.	Pad Name	Typical Value	Note	Reference Command (page)
1	VDDI	1.0uF / 6.3V	I/O and Digital Power	
2	VCI	1.0uF / 6.3V	Analog Power	
3	VSP	2.2~4.7uF / 10V	Analog Power	
4	VSN	4.7uF / 10V	Analog Power	
5	VCORE	2.2uF / 6.3V		
6	VCL	1.0uF / 6.3V		
7	VREG1OUT	1.0uF / 10V	Optional	Register Page 4_R7Ah (page.231)
8	VREG2OUT	1.0uF / 10V	Optional	Register Page 4_R7Ah (page.231)
9	VCOM	2.2uF / 6.3V		
10	VGH	1.0uF / 25V		
11	VGL	1.0uF / 25V		
12	VGLO1	1.0uF / 25V	Optional (if not used)	Register Page 4_R6Fh (page.229)
13	C21P/C21N	1.0uF / 16V		
14	C22P/C22N	1.0uF / 25V	Optional	Register Page 4_R6Fh (page.229)
15	C23P/C23N	1.0uF / 16V		
16	C24P/C24N	1.0uF / 25V	Optional	Register Page 4_R6Fh (page.229)
17	C41P/C41N	1.0uF / 6.3V	Optional	Register Page 4_R6Fh (page.229)
18	C42P/C42N	1.0uF / 6.3V	Optional	Register Page 4_R6Fh (page.229)

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19.5. Maximum Layout Resistance

Table 53: Maximum Layout Resistance

Pad Name	Type	Maximum series resistance	Unit
VCI	Power Supply	5	Ω
VCIREF	Power Supply	10	Ω
VDDI	Power Supply	5	Ω
VCC1	Power Supply	5	Ω
VCC2	Power Supply	5	Ω
VDDAM	Power Supply	5	Ω
VSP	Power Supply	5	Ω
VSN	Power Supply	5	Ω
VSSA	Ground	5	Ω
VSSREF	Ground	10	Ω
LVDSVSS	Ground	50	Ω
VSS	Ground	5	Ω
MTP_PWR	Power Supply	5	Ω
VREG1OUT	Analog	20	Ω
VERG2OUT	Analog	20	Ω
VCL	Analog	5	Ω
VGH	Analog	10	Ω
VGL	Analog	10	Ω
VGLO1	Analog	10	Ω
EXTP	Output	10	Ω
EXTN	Output	10	Ω
LVDSVDD	Analog	5	Ω
VREF	Analog	20	Ω
VCORE	Analog	5	Ω
C21P, C21N, C22P, C22N C23P, C23N, C24P, C24N C41P, C41N, C42P, C42N	Step-up Capacitor	5	Ω
IM[2:0], RS[1:0] LANSEL, BOOSTM[2:0]	Input	100	Ω
RESX	Input	100	Ω
TE, TE1, LEDPWM	Output	50	Ω
CLKP, CLKN D1P, D1N D2P, D2N D3P, D3N	Input	5	Ω
D0P, D0N	Input + Output	5	Ω
CSX, DCX, SCL, SDI	Input	100	Ω
SDO	Output	100	Ω
GOUT_L[22:1] GOUT_R[22:1]	Output	10	Ω
VCOM	Analog	5	Ω
VTESTOUTP	Analog	100	Ω
VTESTOUTN	Analog	100	Ω
TOUT[3:0]	Input + Output	100	Ω
TEST[5:0]	Input + Output	100	Ω
VS, HS	Input + Output	100	Ω
PCLK	Input	100	Ω
D[7:0]	Input + Output	50	Ω

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20. Liquid Crystal Power Supply Specifications

Table 54: Liquid Crystal Power Supply Specifications

Item		Description
TFT Source Driver		2404 pins , 800(RGB)
TFT Gate Driver Control Signal		44 pins
TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
Liquid Crystal Drive Output	S1 ~ 2400, SDUM[3:0]	V0 ~ V255 grayscales
	GOUT_L/R[22:1]	VGH – VGL
	VCOM	-4.0 ~ -0.2V; 0V
Input Power Voltage	VCI	2.50 ~ 6.6V
	VCIREF	2.50 ~ 6.6V
	VDDI	1.65 ~ 3.6V
	VCC1	1.65 ~ 6.6V
	VCC2	1.65 ~ 6.6V
	VDDAM	1.65 ~ 3.6V
	VSP	4.5 ~ 6.6V
	VSN	-6.6 ~ -4.5V
Liquid Crystal Drive Voltages	VGH	8.0V ~ 18.0V
	VGL	-18.0V ~ -7.0V
	VCL	-3.0V ~ -2.3V
	VGH – VGL	Max. 32.0V
Internal Step-up Circuits	VGH	2xVSP or 2.5xVSP or 3*VSP or 3.5*VSP or 4*VSP or 4.5*VSP or 5*VSP
	VGL	-1.5xVSP or -2xVSP or -2.5xVSP or -3xVSP or -3.5xVSP or -4xVSP or -4.5xVSP or -5xVSP

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21. Revision History

Version No.	Date	Page	Description
V098	2015/11/11	All	New created
V099	2016/01/08	181 282	Modify Page1_R02h Modify Rise time
V100	2016/03/15	284	Modify Power on/off sequence
V101	2016/05/13	288	Modify External MTP_PWR Programming Flow
V102	2017/03/16	18 304	Delete 640 (RGB) (H) x (480 + (4 x NL) (V) resolution Modify High Speed Mode to Low Power Mode Timings

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